Design as You See FIT: System-Level Soft Error Analysis of Sequential Circuits

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Soft errors in VLSI circuits

- Spurious radiation-induced flip of one or more stored bits
- Does not permanently damage devices
- Measured in units of FIT; 1 FIT is 1 failure in 10^9 hrs
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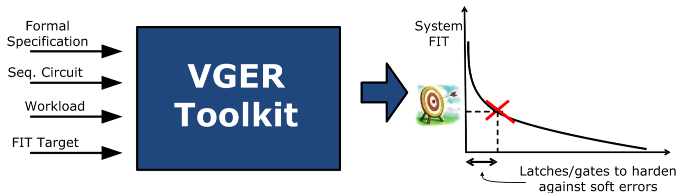
- Logic FIT may increase 9 orders of magnitude from 1992-2011 [Shivakumar 02]
- Logic FIT approaching memory FIT around 100nm [Shivakumar 02, Baumann 05]

Circuit-level hardening techniques exist, but have costs

Our contribution

the verification guided error resilience methodology

- Use formal specifications to capture system-level correctness



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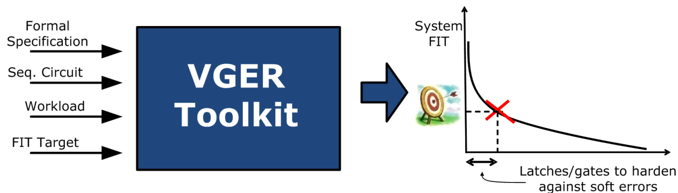
- Use verification to analyze system-level impact of circuit-level upsets



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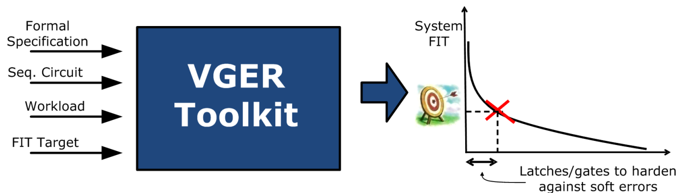

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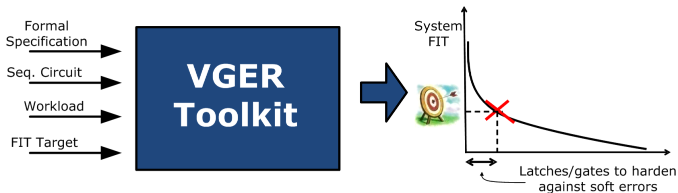
Particularly suited for communication protocols and on-chip networks



Outline

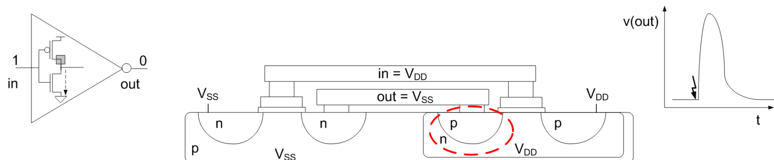
Introduction
- Single Event Upset
- Circuit-level masking
- System-level masking

VGER Toolkit
- BFIT: Circuit-level soft error analysis
- Sequential Simulation with Monitors

Case Study: CMP Router
- Analysis
- Efficient Hardening

Basic mechanisms of single event upset (SEU) in logic

- Strike near sensitive diffusion
  - Sensitive diffusion is a function of gate input
  - If sufficient charge, glitch results at gate output
  - Glitch propagates downstream toward sequential element(s)



Circuit-level masking

not all glitches are equally likely to flip bits

Logical Masking

- Is there a sensitized path from strike to latch(es)?

Timing Masking

- Does the glitch arrive at latch(es) while open?

Electrical Masking

- Is the strike magnitude sufficient to cause upset?

SEU can lead to single (SBU) or multi-bit upset (MBU)

Circuit-level masking

Related work

Circuit-level masking

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- Static analysis of circuit structure [Miskov-Zivanov 06, B. Zhang 06]

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Our approach

- An efficient method for estimating electrical/timing masking
  - Analysis of circuits up to 20k gates
  - Able to handle multiple sensitized paths
  - Analysis of both SBU and MBU

System level masking
not all bit flips are equally likely to cause system failure

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- Architectural Vulnerability Factor [Mukherjee 03]
  - Find probability of a bit flip leading to incorrect future execution
  - Requires detailed architecture model

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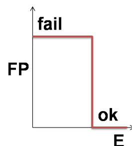
- Verification Guided [Seshia 07]
  - Find ~~probability~~ possibility of a bit flip leading to bad behavior
  - Bad behavior formalized using specifications
  - Model checking identifies non-critical latches
  - High confidence but binary
  - Can apply to individual functional blocks



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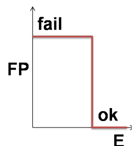

Our approach

- Verification guided, but produce a refined ranking

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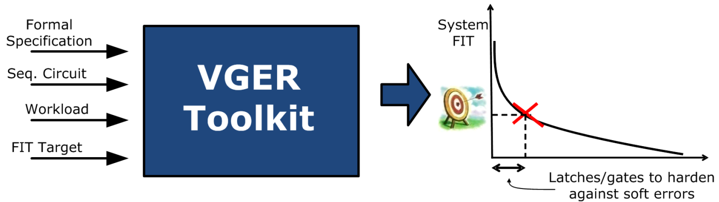
VGER toolkit



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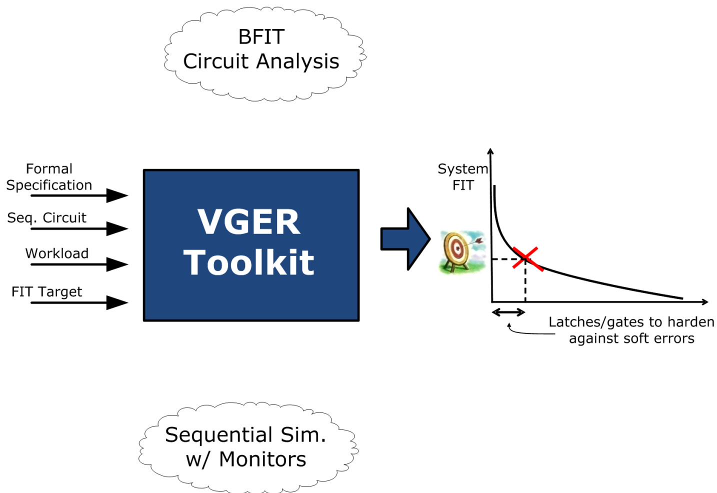

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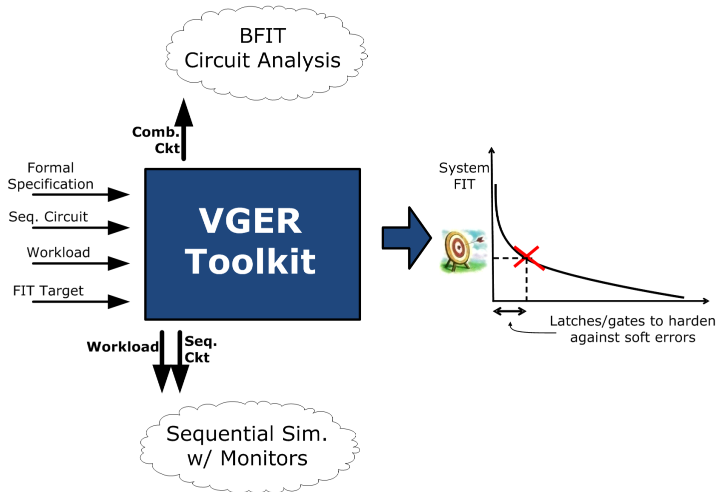

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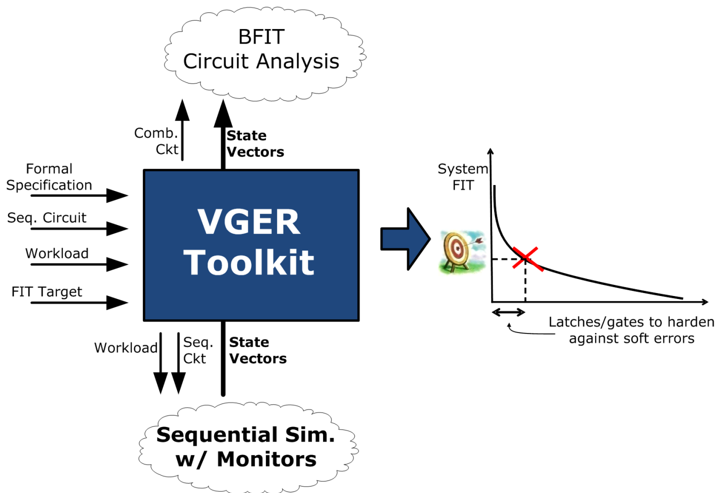

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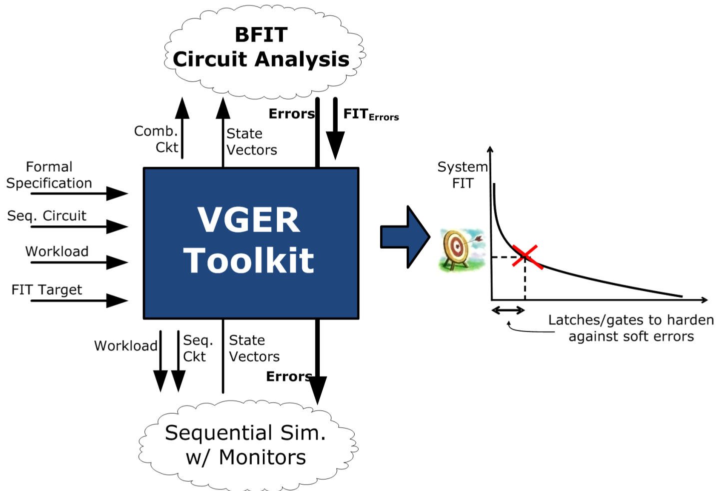

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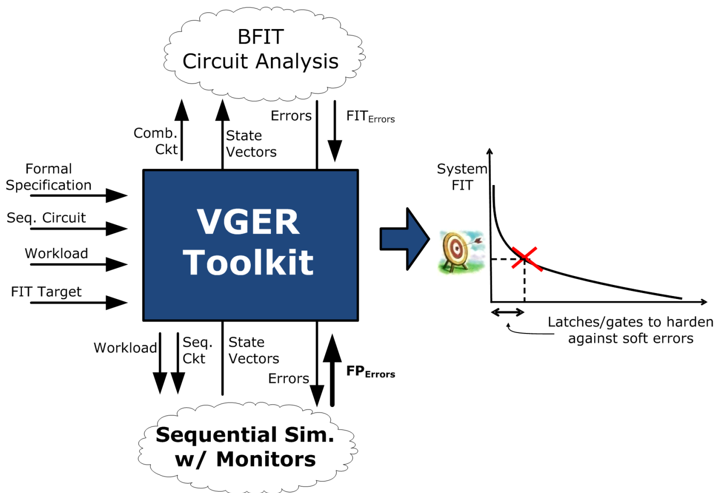

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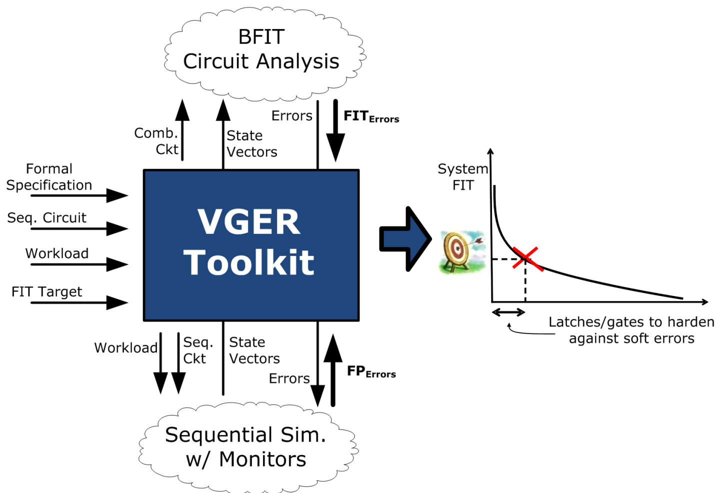


BFIT circuit level analysis tool

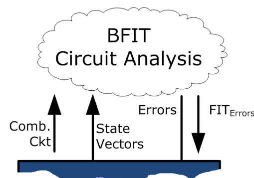
- Open source C++ simulation tool for combinational logic circuits
- Based on Nangate 45nm open cell library

Inputs

- Comb. circuit and sampled states

Outputs

- FIT of all events: $FIT_{g \rightarrow E}$
  - Struck gate g
  - Set of upset sequential elements E
  - some E are SBU, others are MBU



What determines the FIT of an event?

- Every possible strike is represented by a collected charge and time (q, t)

$$FIT_{g \rightarrow E} \propto \int \int R_g(q,t) \, N_{g \rightarrow E}(q,t) \, dt \, dq$$

$R_g(q,t) \in \Re$

probability of observing strike q, t at gate g

$N_{g \rightarrow E}(q,t) \in \{0,1\}$

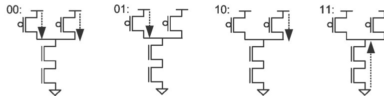
conditional probability of upset in set E of latches, given a strike q, t at gate g

  - **Encompasses logical, electrical, timing masking**

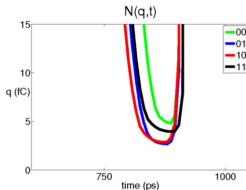
BFIT approach to Masking

$N(q, t)$ of single path can be characterized using path delay and gate input

- Inputs determine drive strength



- Input determines shape of $N(q, t)$



00	01	10	11
5.0E-6	7.5E-6	16.1E-6	2.9E-6

Table: FIT vs gate input

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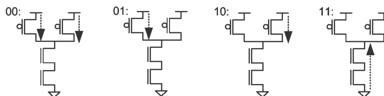

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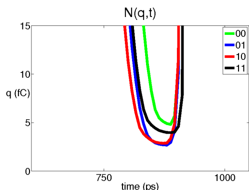

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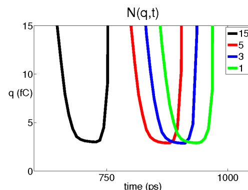
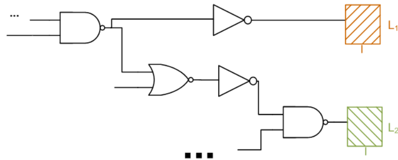
- Path delay is time-shift to $N(q, t)$



15	5	3	1
6.2E-6	6.4E-6	6.4E-6	6.7E-6

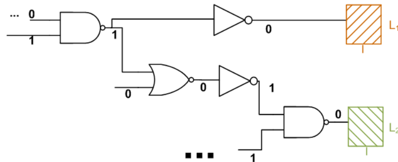
Table: FIT vs path length

Demonstration of BFIT algorithm



Demonstration of BFIT algorithm

1. Forward propagate input vector in levelized DAG



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1. Forward propagate input vector in levelized DAG
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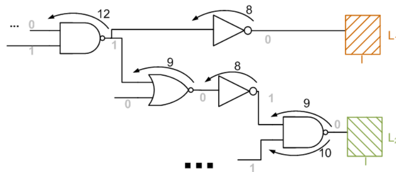
   - If an input can flip current gate, back propagate delays



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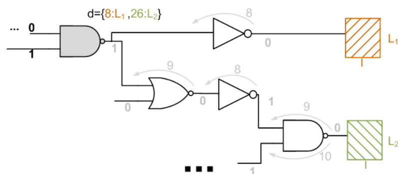
   - Cell precharacterization



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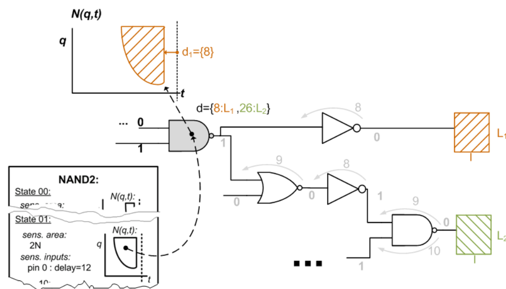

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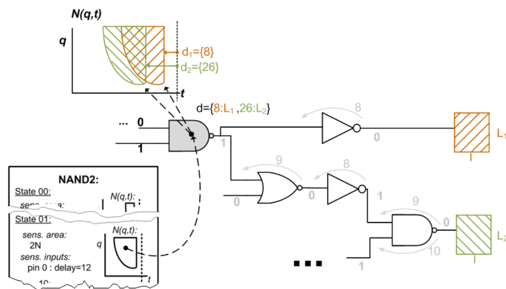
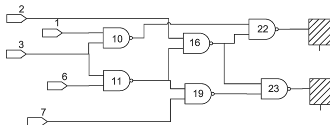
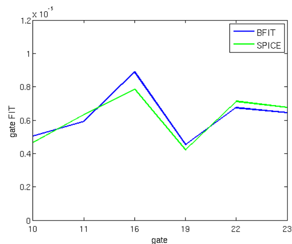


BFIT results





Circuit	INPUTS	LATCHES	GATES	RUNTIME (s/1k vectors)	FIT
s5378	214	179	3232	35	3.27e-3
s9234	247	228	7230	68	1.06e-2
s13207	700	669	10277	136	1.77e-2
s15850	611	597	12712	207	2.24e-2
s38417	1664	1636	28223	451	5.62e-2
s38584	1464	1452	28854	1311	4.85e-2
s35932	1763	1728	23012	204	3.99e-2

BFIT results
multiple bit upsets

- Do MBU occur?

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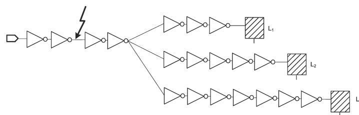

	BFIT	HSPICE
SBU	8.6e-7	7.4e-7
MBU	9.0e-7	12.6e-7
total FIT	1.7e-6	2.0e-6

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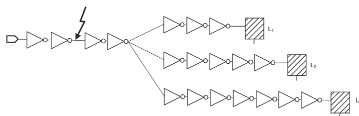

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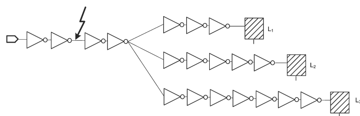

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Circuit	%SBU	%MBU
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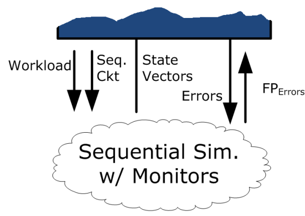
s9234	0.8625	0.1375
s13207	0.9379	0.0621
s15850	0.9148	0.0852
s38417	0.8812	0.1188
s38584	0.9538	0.0462
s35932	0.9960	0.0030

Verification Guided Error Resilience
using sequential simulation with monitors

- Correctness captured in specifications
- Hardware monitors synthesized from specifications
- Estimate failure probabilities using random fault injections
- Accurately incorporate workload
- Produces refined ranking

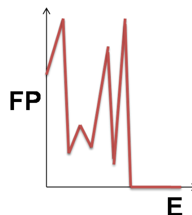


Inputs

- List of formal specifications
- List of circuit errors E

output

- FP_E - the probability that upset E will lead to a violated specification



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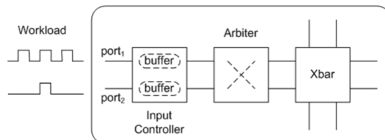
Chip Multiprocessor (CMP) Router



- Simplified 2 port version of 5 port design[Peh 01]
- 174 latches, ≈1300 gates

Specification

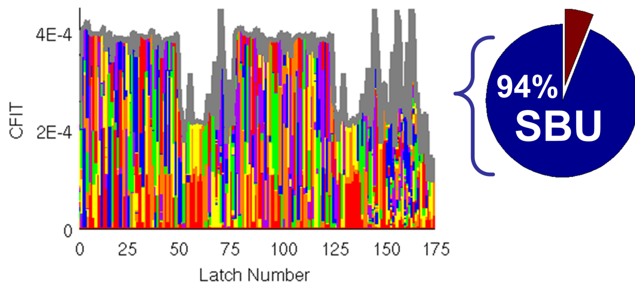
Every incoming flit must be routed correctly within 11 cycles

Target

Select gates or latches to harden to reduce combinational FIT to FIT_{TARGET}

BFIT analysis of CMP router

- Output from BFIT tool:



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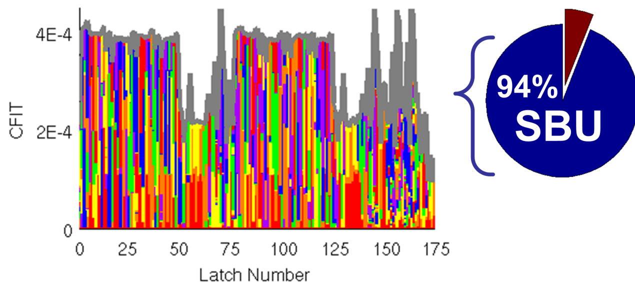

- Thousands of E observed, but over 94% are SBU

System level masking in CMP

94% of SEU are SBU

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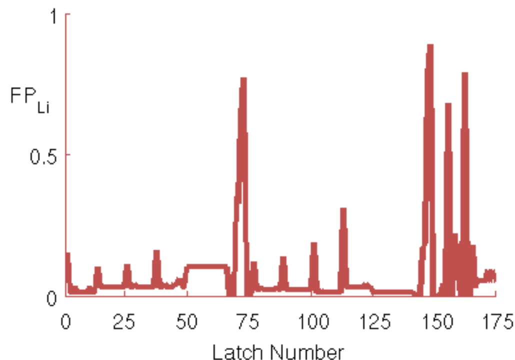
- Find failure probability (FP_E) for all SBU



CMP - all masking factors

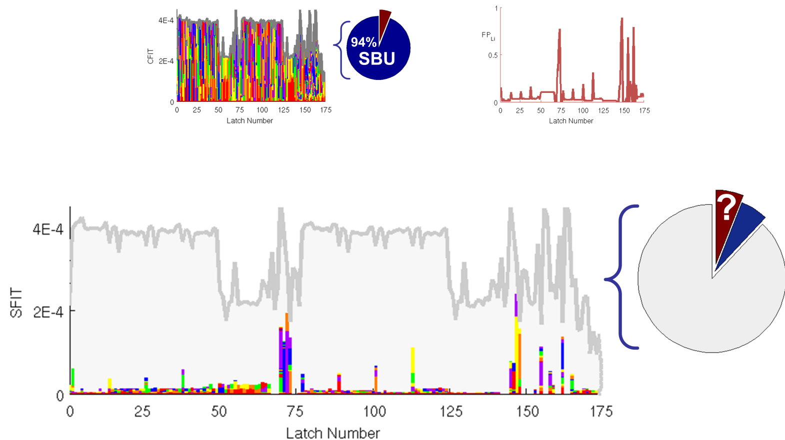


Figure: System-level SBU FIT

CMP
Achieving FIT target by hardening gates or latches

Hardening gates

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Hardening gates

Assume a hardened gate contributes no FIT

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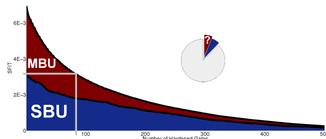
- To achieve $FIT \leq FIT_{TARGET}$:
  - Harden 81/1300 gates



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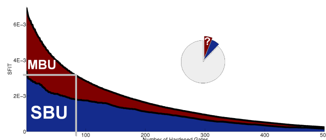


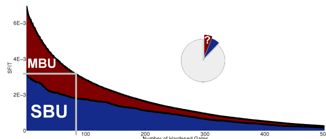
- Pareto optimal coverage if all MBU causes system failure

CMP
Achieving FIT target by hardening gates or latches

Hardening gates

Assume a hardened gate contributes no FIT

- To achieve $FIT \leq FIT_{TARGET}$:
  - Harden 81/1300 gates



- Pareto optimal coverage if all MBU causes system failure

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CMP
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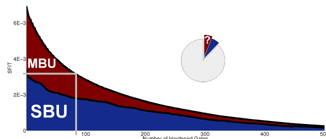

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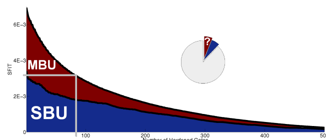

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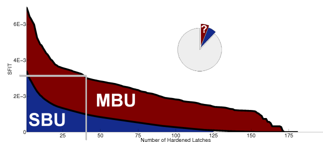

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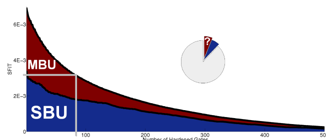

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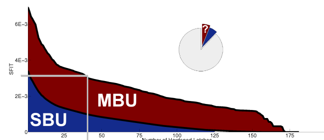

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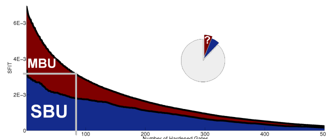

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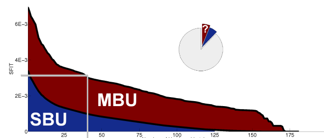

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. . . design as you see FIT

Summary

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- Can guide cost-effective hardening of circuit level features
- Provide designer flexibility to harden either gates or latches
- MBU poses threat to reliability

Thank You

BFIT

is available at `www.eecs.berkeley.edu/~holcomb/bfit.htm`

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