

Industrial Outreach

Edited and Presented by
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Chess Review
November 18, 2004
Berkeley, CA



Industrial Advisory Board



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- Theo Claasen, (CTO, Philips)
- Andrea Cuomo (Senior VP Strategy and General Manager, Advanced System Technology, ST)

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Tools

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- Bran Selic (CTO, Rational Technology (IBM))
- Ted Vucurevich (CTO, Cadence)

Overview



- Escher
- Industrial use of Metropolis
 - Automotive (Daimler-Chrysler, GM, Toyota)
 - Multi-media and Wireless (Infineon, Intel, Sony, ST, Xilinx)

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**Corporate
Customers**

Government

ESCHER

Research Groups

Mission: Non profit organization to provide services that promote the transition of government-funded Information Technology research and Development results to industry

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Strategic Objectives



- **Preserve, maintain and mature** the fruits of government research investments
- Build a **research infrastructure** for selected technology areas (initial focus has been distributed embedded systems)
- Enable **leveraging** of the technological infrastructure across industrial sectors (such as automotive, aerospace, space systems, medical devices and manufacturing automation)
- **Identify research needs**, serving as a "voice of the customer" (VoC) to researchers and government agencies funding research
- **Identify development needs** and requirements, serving as a "voice of the customer" (VoC) to providers of solution technologies and tools
- Be available as a **resource** for knowledge and other share-able resources to American researchers, developers and users



Business Model



- Stage 0:**
- Road mapping and other consulting services
- Stage I:**
- Participation in government program to work with specific performers - funded by program
 - Quality standards create goal and possible corporate follow on for performers create positive incentives
 - Software is not lost if not transitioned at end of program, but becomes "GFE" for the next stage
 - Escher helps with license issues
 - Funding credit tag remains with technology for future tracing
- Stage II:**
- Corporate funding to mature/harden/complete/customize research results
 - Escher coordinates the project - pooled funding and joint performers
 - Feedback to government funding agencies





Escher Structure



- **Structure:** 501(c)(3) Non-profit Research Institute
- **CEO:** Dr. Norm Whitaker
- **Initial Funding**
 - **Corporate:** General Motors, Raytheon, Boeing
 - **Government:** National Science Foundation, DARPA,
- **Initial Focus:** Infrastructure for Embedded System Design
- **Initial Board of Directors**
 - Prof. Janos Sztipanovits - Vanderbilt U
 - Prof. Shankar Sastry - UC Berkeley
 - Prof. Doug Schmidt - Vanderbilt U



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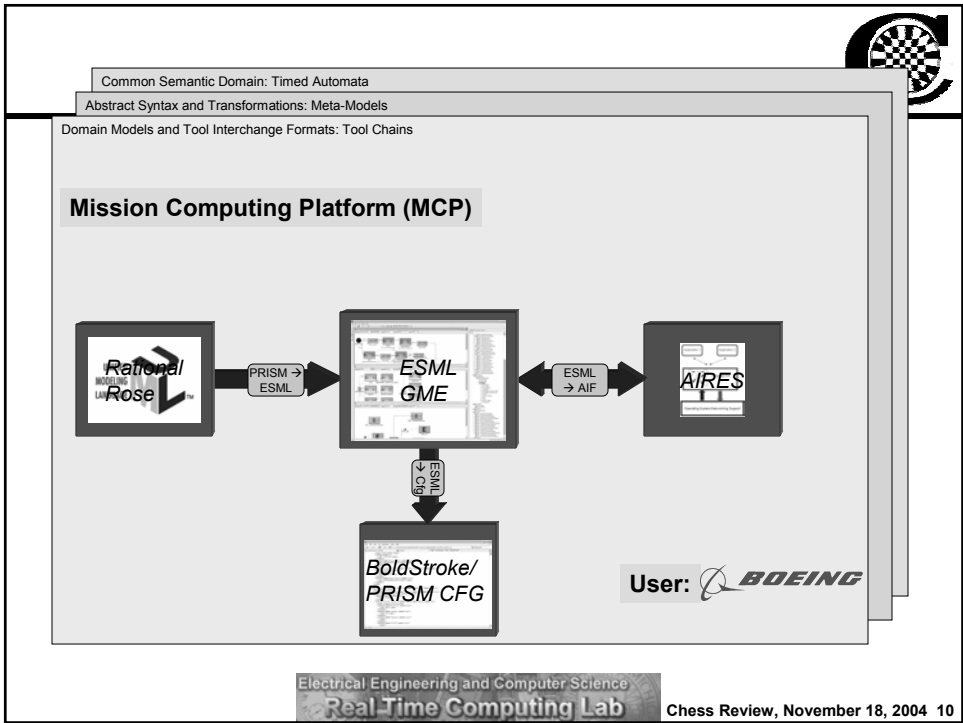
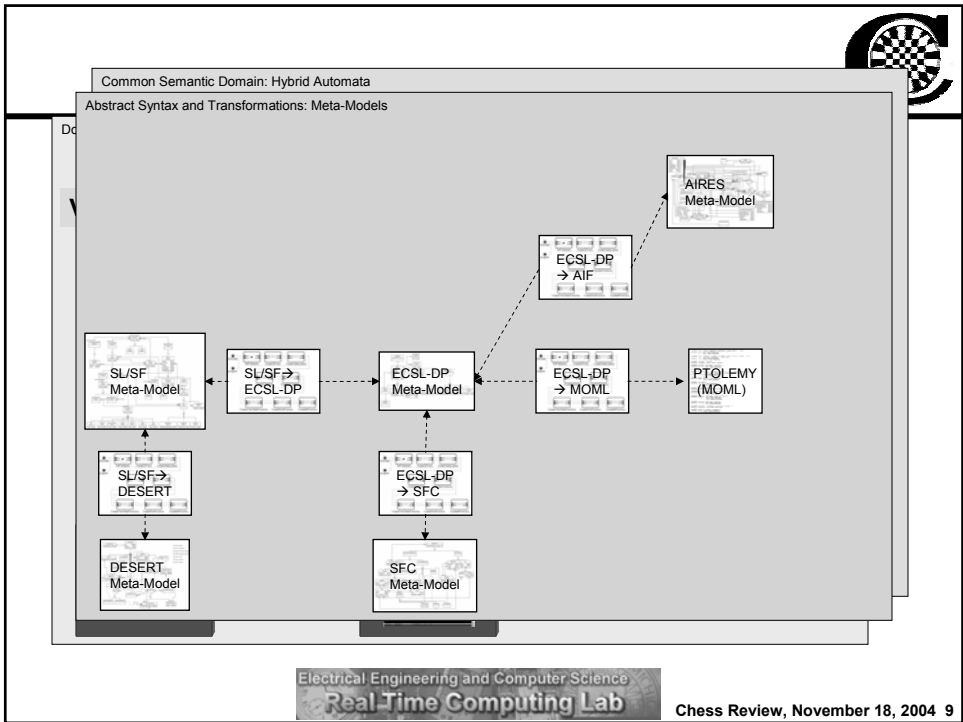
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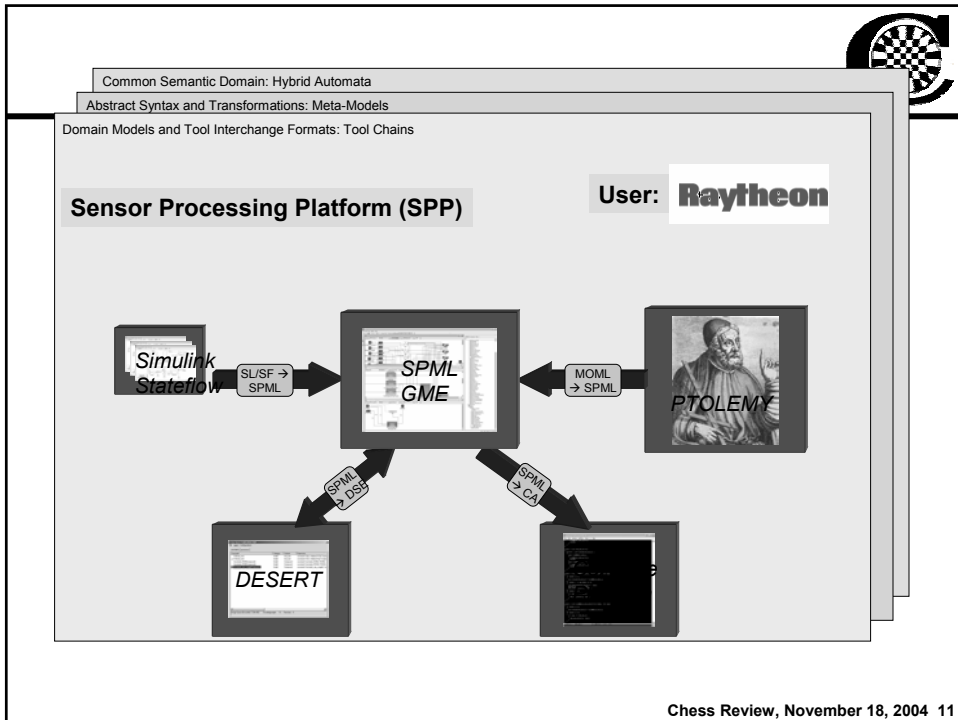


- Incubation completed, ESCHER has been incorporated in February 2004
- VU-ISIS span out ESCHER an independent entity in March, 2004
- Year 1 work progresses under direction of the Technical Advisory Board (TAB) (Boeing, GM, Raytheon)
- In May, 2004 the Tab finalized FY04 technical schedule, which includes:
 - Initial Repository Setup
 - Three tool chains using U. Michigan, Berkeley and VU-ISIS tools
 - Training programs for industry
- In November 2004, TAB gave the "go-ahead" for Year 2



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- ## Overview
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Metropolis: an Environment for System-Level Design



- Motivation
 - Both design complexity and the need for verification are increasing
 - Semantic link between specification and implementation is necessary
- Platform-Based Design
 - Meet-in-the-middle approach
 - Separation of concerns
 - Function vs. architecture
 - Capability vs. performance
 - Computation vs. communication
- Metropolis Framework
 - Extensible framework providing simulation, verification, and synthesis capabilities
 - Easily extract relevant design information and interface to external tools
- Released Sept. 15th, 2004

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Metropolis Contributors



Industry

- Cadence Berkeley Labs (Design Methods and Tool Development)
- General Motors (Distributed subsystems)
- Infineon (Platform-based cell phone design)
- Intel (Wireless platforms, Imaging-Video subsystems)
- National Semiconductors (Analog Platforms)
- ST (Set-top box, Automotive, Sensor Networks)
- United Technologies (Air conditioning, Security)

Universities

- University of California at Berkeley
- Carnegie Mellon University
- Politecnico di Torino
- Scuola di Sant'Anna (Pisa)
- Universita' de L'Aquila
- Universita' di Trento
- UCLA
- UC Riverside
- Universitat Politecnica de Catalunya

Consortia

- BWRC (Cadence, HP, Ericsson, Infineon, Intel, Nokia, Qualcomm, ST, ...)
- PARADES (Cadence, Magneti-Marelli, ST, UTC)

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Highlights



We studied **36** different architectures for IFX-3 Concept Car (HyWire System) within the context of differing:

- Network architectures
- Software architectures
- Node architectures

- Entire design cycle completed from March 26th to May 15th
 - Static analysis tools can return results within minutes
 - Bottleneck is preparing format for entering the tool chain

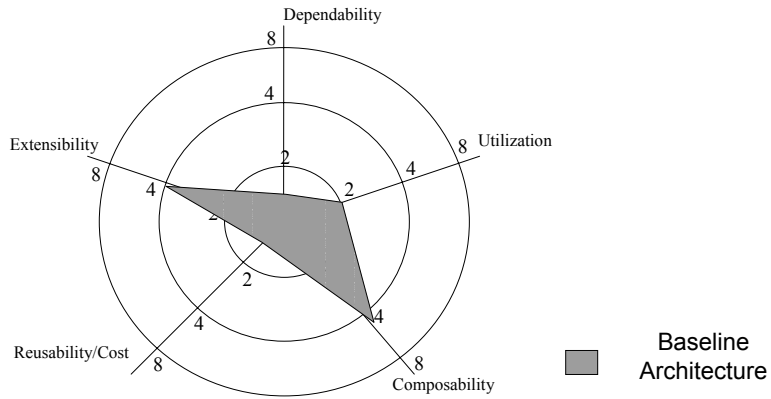
- Three people involved on a part-time basis (< 50%)
 - Sri Kanajan
 - GM Researcher
 - Claudio Pinello
 - PhD student at UC Berkeley (now at Quantech GM Berkeley Labs)
 - Paolo Giusto
 - SysDesign Expert (now at Quantech GM Berkeley Labs)

SBW Architecture Development: Metrics

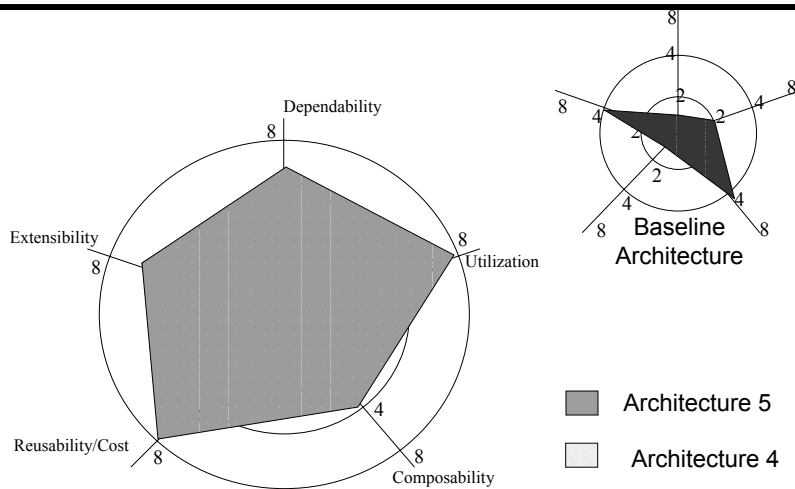


- Dependability/Fault Tolerance [failures/hour]
 - Reliability and availability → failure rates
- Utilization [% of resource bandwidth usage]
 - Processor and bus utilization
- Reusability/cost [number of unique components]
 - This is defined as how much of the architecture can be made common.
- Extensibility [% of remaining "space" for future extensions]
 - This is defined as the ability to extend the current architecture in terms of functionality or hardware configuration without causing "coordinated" change.
- Temporal Composability [Degree of synchronization between components]
 - This is defined as the ability to integrate components together without loss of the original properties of the individual components.

Architecture 1 Baseline: Result Representation



Architecture 5: Result



Summary



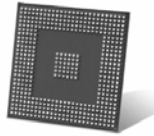
- **Steer-by-Wire Sub-system analysis**
 - Qualitative and quantitative metrics introduced
 - 36 fault tolerant architectures analyzed in 1.5 months
 - Significant architecture improvements in comparison to baseline
- **Automotive Architecture Exploration Tool Chain**
 - **Metropolis (UC Berkeley)**
 - Specify, analyze, and synthesize systems at several levels of abstraction
 - **SysDesign (Cadence)**
 - Simulation tool that bridges pure functional modeling and architecture design
 - **SCRAPE (UC Berkeley)**
 - Fault Tolerant Design Exploration and Synthesis
 - Worst case static analysis tool

Overview



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Metropolis in the Multimedia Domain



(Intel MXP5800 and Xilinx Virtex-II Pro)

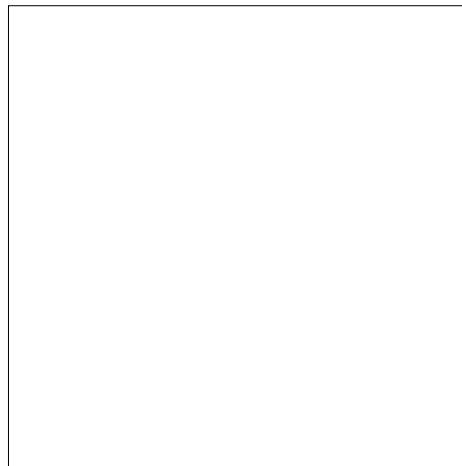


- Case studies involve concurrent, heterogeneous, and reconfigurable architectural platforms
- Applications are typically data intensive streaming applications
 - Kahn Process Networks is a common model of computation
- Mapping must take into account:
 - Computation (due to heterogeneous arch. platforms)
 - Communication (due to application characteristics and platform concurrency)

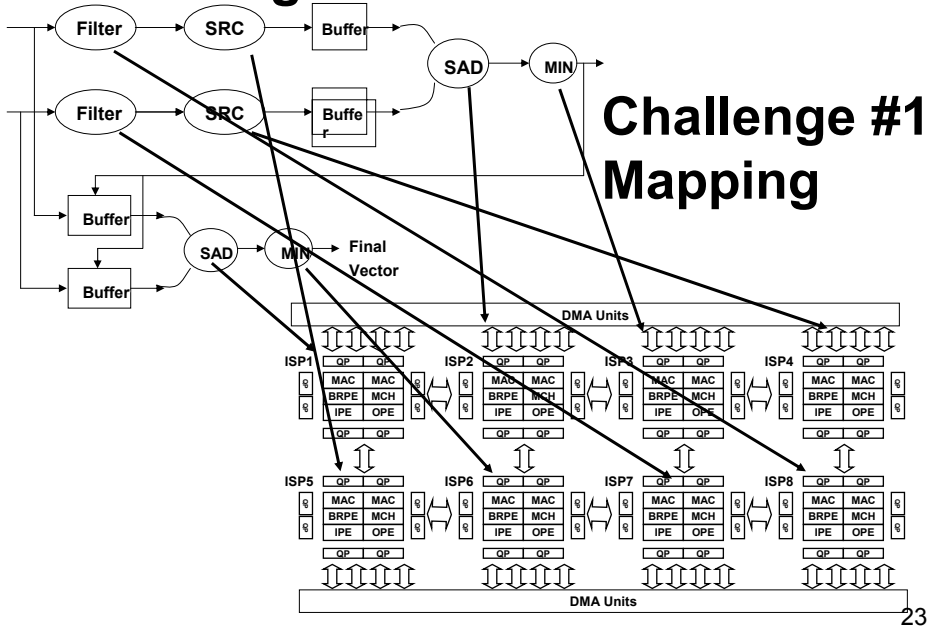
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Typical Application: The Intel MXP5800

- **Complete Solution for high performance Digital Imaging Applications**
 - Multifunction Printers
 - High End scanners



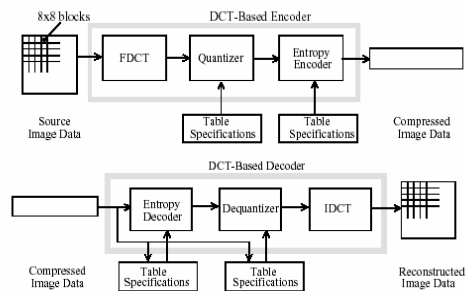
Challenge for Platform Reuse



Intel Project Overview



- Initially explore mapping of JPEG encode/decoder application
- Choose the abstraction level and mapping strategy such that results correlate with actual implementation




From: G. K. Wallace, The JPEG Still Picture Compression Standard

Xilinx Collaboration



- Create a flow to characterize performance of Xilinx designs.
- Create **Metropolis Models** of Xilinx CoreConnect Components
 - Create models of architectural families based on overall topology of components.
 - Various abstraction levels
 - Tie into the EDK flow for implementation
- Produce **Metropolis Functional Model** of well examined application using Xilinx HW
 - JPEG2000 strong candidate
- Enhance mapping infrastructure to support the co-simulation of such models.
- Examine the results of the co-simulation and characterization in order to draw conclusion regarding design space exploration of Xilinx based designs in Metropolis.

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Never stop thinking

Proposal for Common Framework for Cognitive Radios

function modeling

- WCDMA, DVB-H, UWB,
- WLAN, WIMAX, ...
- CR

front-end for code generators

back-end

back-end

back-end

architecture modeling

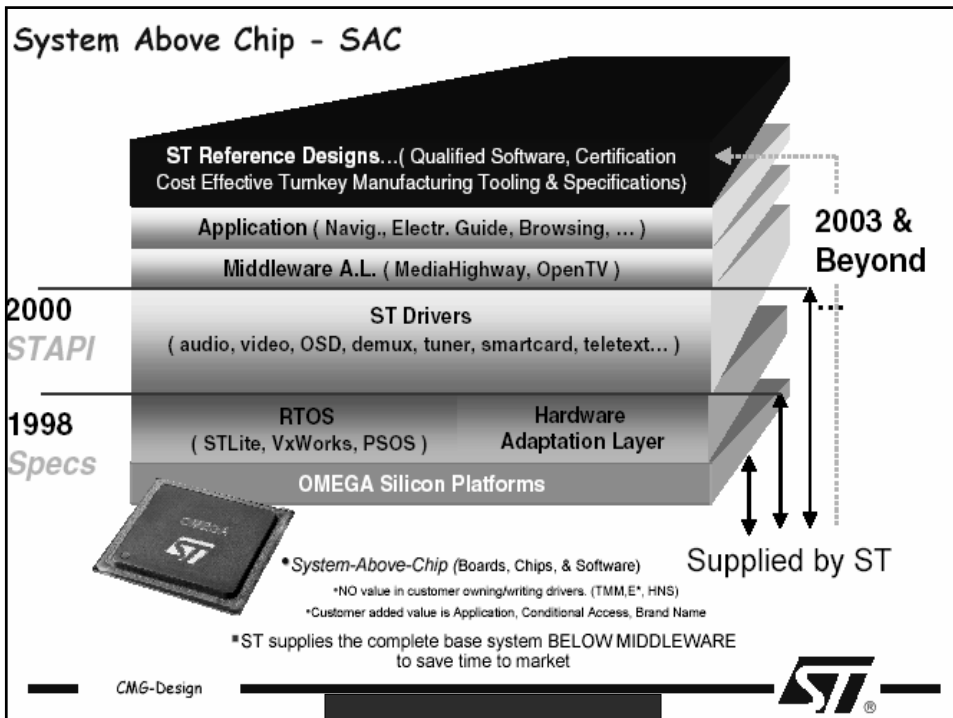
- multiple program-
mable processors

- reconfigurable DP+IC
architecture

- fpga-inspired
architectures

Common Research Agenda:

- benchmarks
- real-time in f&a space
- common rules for modeling
- connection between function and architecture model
- systematic design space exploration
- synergy in designing code generators
- „Future-proof“ framework for Function&Architecture Modeling (Matlab, Simulink, **Metropolis**)



Concluding Remarks



- Rich interaction with industry
- Different domains addressed: IC, Systems (e.g., Automotive, Avionics, Defense, Consumer), Tools
- Impact on research agenda and on product development
- Escher provides a wealthy model to support and distribute results from our research to maximize impact both ways
- Escher complements and extends traditional approach to industrial interaction and tool distribution tested for years at Berkeley