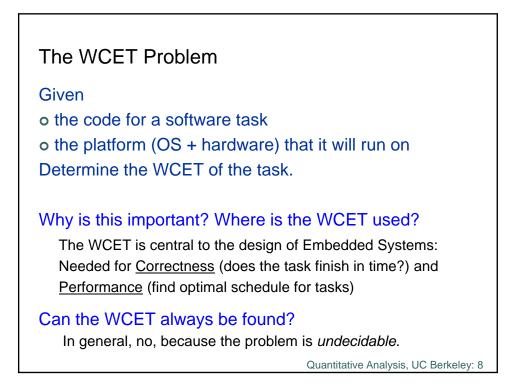
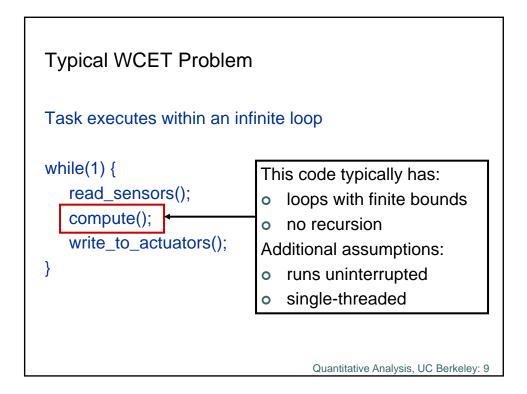
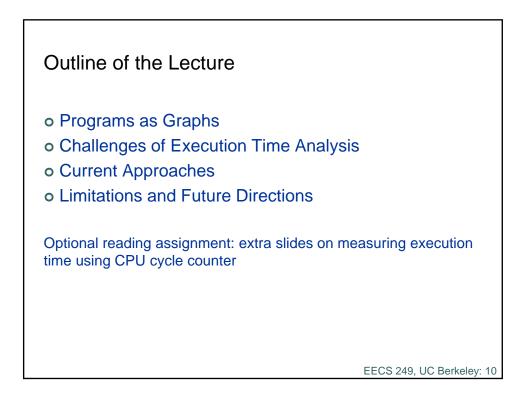
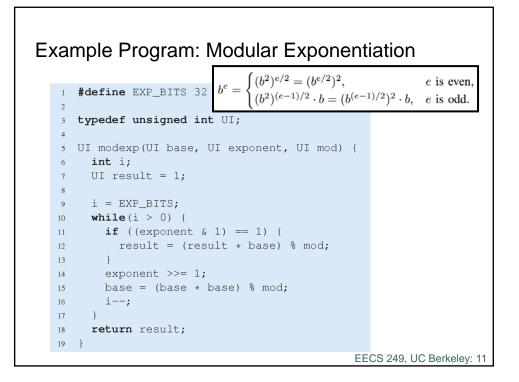


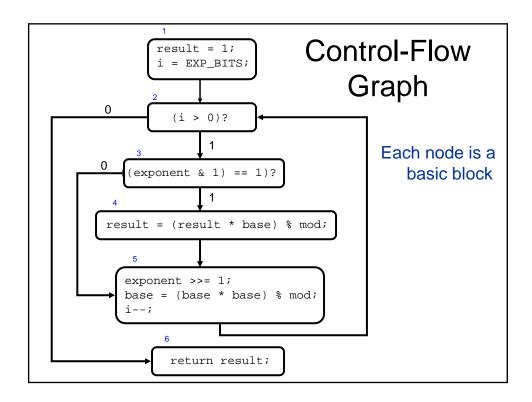
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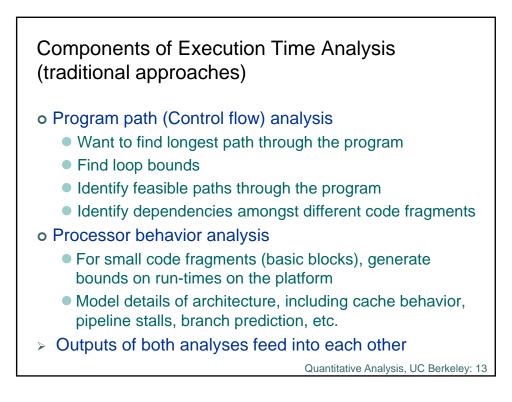


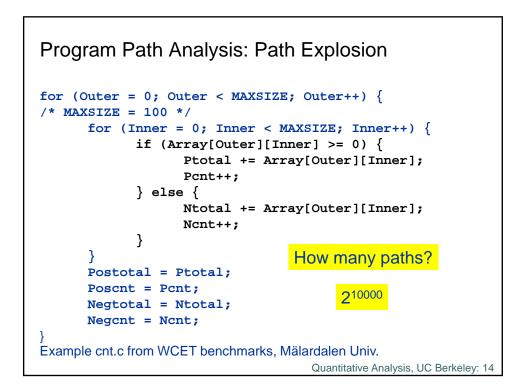


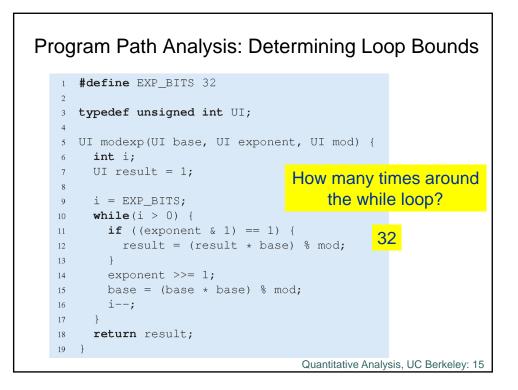


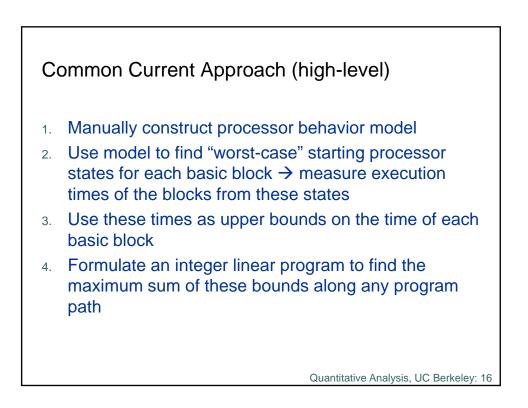


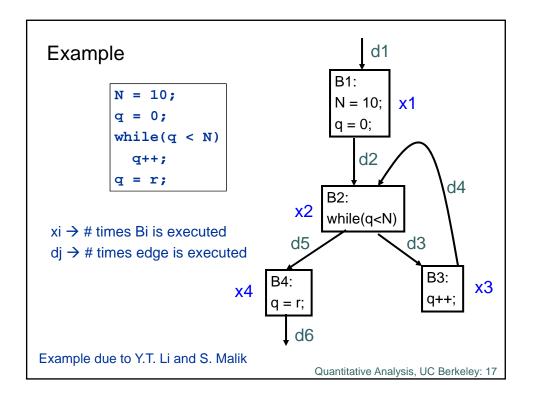


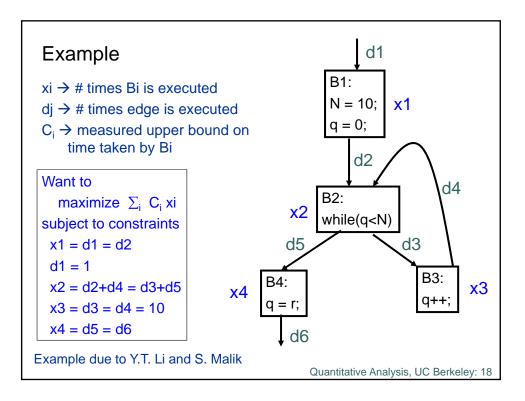


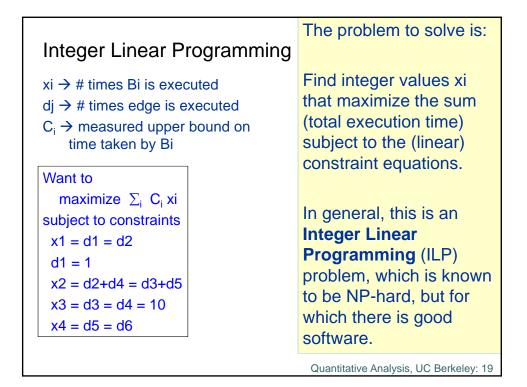


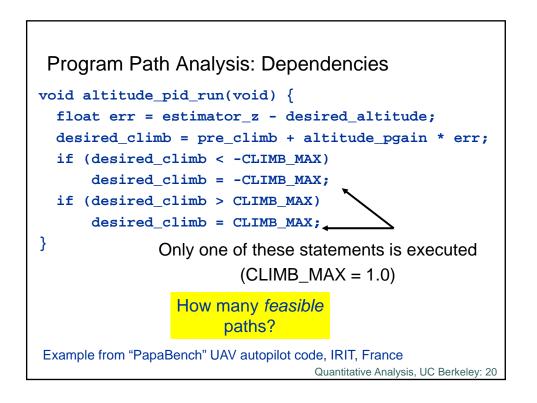


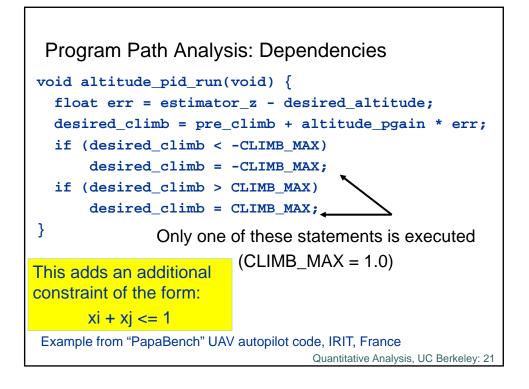


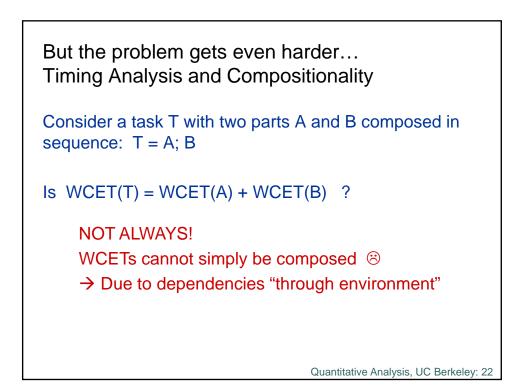


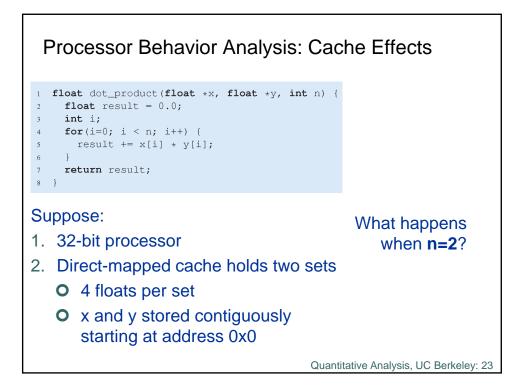


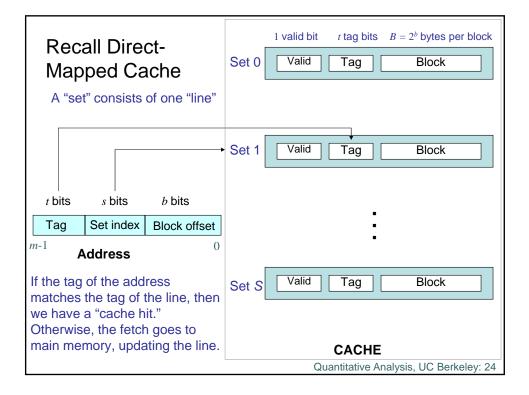


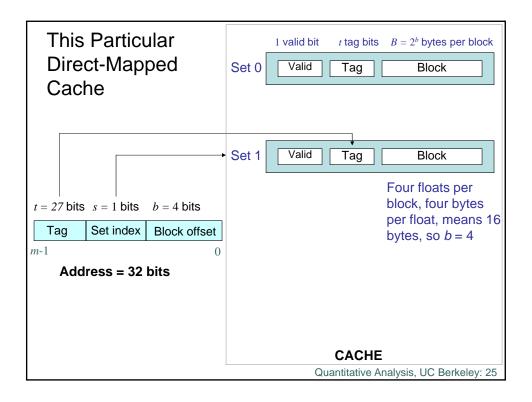


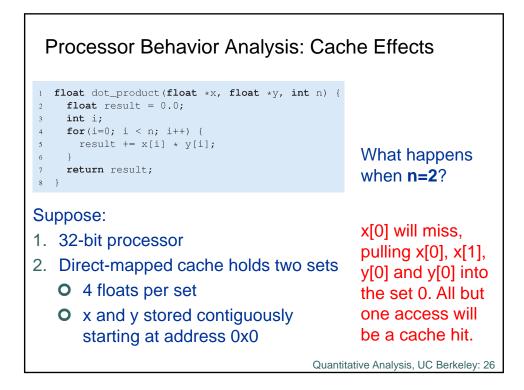












Processor Behavior Analysis: Cache Effects What happens float dot_product(float *x, float *y, int n) { float result = 0.0; when **n=8**? int i; for(i=0; i < n; i++) {</pre> x[0] will miss, result += x[i] * y[i]; pulling x[0-3] into return result; } the set 0. Then y[0] will miss, Suppose: pulling y[0-3] into 1. 32-bit processor the same set, 2. Direct-mapped cache holds two sets evicting x[0-3]. Every access will **O** 4 floats per set be a miss! • x and y stored contiguously starting at address 0x0 Quantitative Analysis, UC Berkeley: 27

