Network Time Synchronization with IEEE 1588
(Time Distribution in Embedded Systems)

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Agenda

1. Major time distribution systems used in embedded systems
2. How, where and why they are used
3. Application examples
4. Time distribution- in particular IEEE 1588- as an embedded system

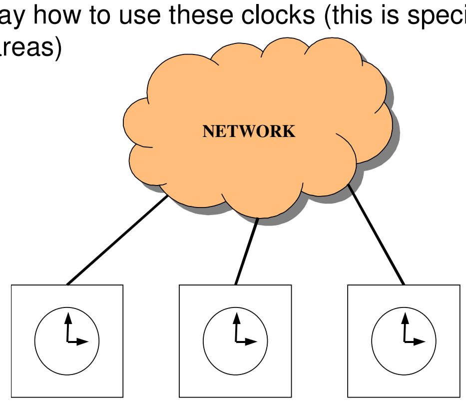
Major time distribution systems used in embedded systems

1. NTP- c <1985, ~10ms
2. GPS- c 1972, operational in 1993,~100ns: (Glonass, Galileo)
3. IRIG-B- c 1960, ~1-10 us
4. IEEE 1588-2008 – c 2002, ~20ns on Ethernet
5. Proprietary or controlled protocols, e.g. FlexRay(c ~2000), TTP(c ~1993), TTE(c ~2005)…

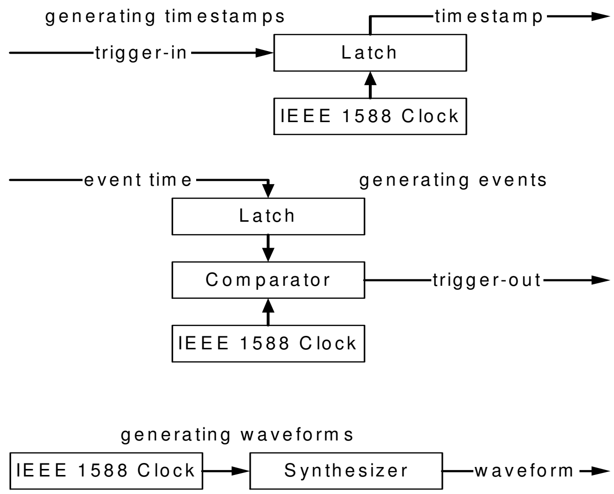
Purpose of IEEE 1588

IEEE 1588 is a protocol designed to synchronize real-time clocks in the nodes of a distributed system that communicate using a network

- It does not say how to use these clocks (this is specified by the respective application areas)



Coupling IEEE 1588 to your application (This is your job- the standard has no opinion on how it is used)

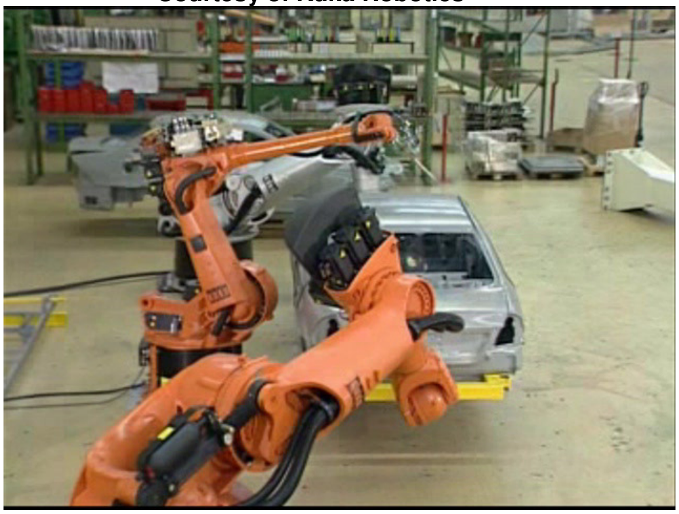


Where is IEEE 1588 being (or likely to be used)?

1. Power generation (>50K nodes in service)
2. Industrial automation (esp. motion control)
3. Telecom (cellular backhaul initially- already field installations)
4. Audio visual systems (as IEEE 802.1AS a specialization of 1588)
5. Military, aerospace, instrumentation (flight qualification, surveillance, data acquisition)
6. Other nascent applications

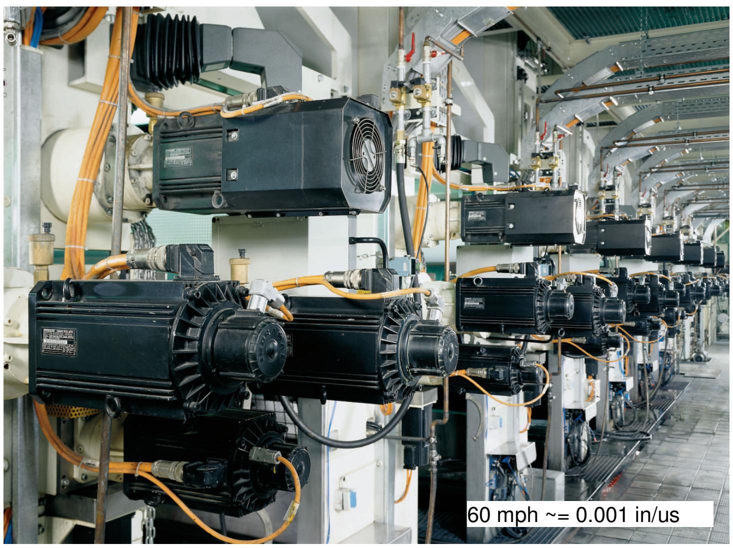
RoboTeam in Action: Process Relative Motion

Courtesy of Kuka Robotics

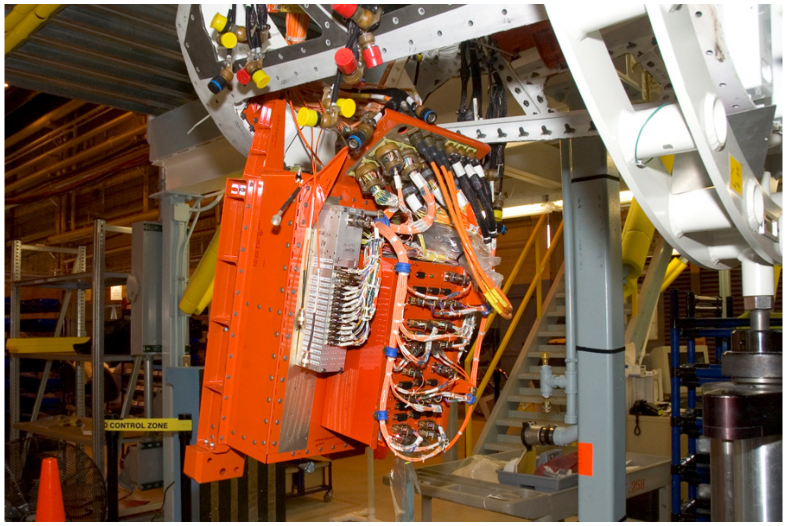


e.g. high speed printing

Courtesy of Bosch-Rexroth.



IEEE 1588 enabled flight test instrumentation in the forward fuselage of a test aircraft. (Data acquisition)



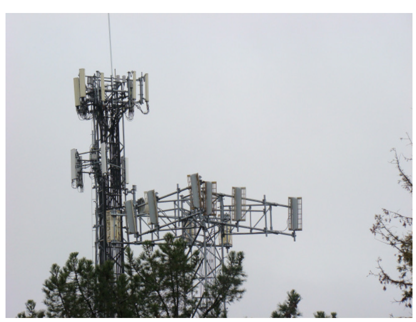
Courtesy of Teletronics

Telecommunications Applications

<u>Cellular backhaul is the major telecom application to date</u>. Metro-Ethernet in field trial. Femtocells beginning.

Companies involved (partial list):

- Nokia-Siemens, Brilliant, Semtech, Zarlink, …



Power System Applications

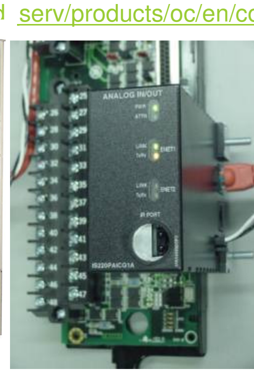
IEEE Power System Relaying Committee (PSRC) recently approved formation of Working Group H7 "IEEE 1588 Profile for Protection Applications"

Power System Applications

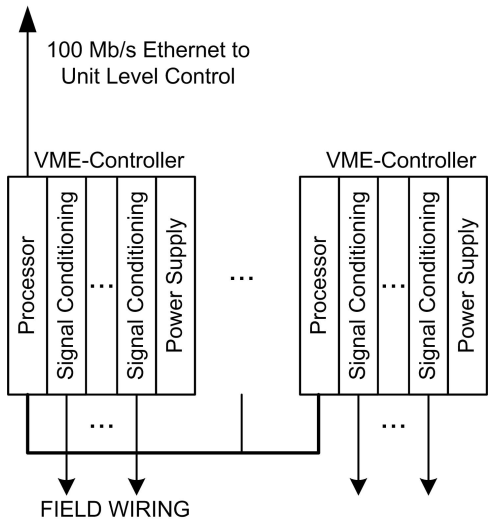
(Courtesy of General Electric)

GE uses 1588 in the Mark™VIe control system for large generators, turbines, wind farms, and other DCS applications. (>50K I/O Packs with 1588 shipped to date)

http://gepower.com/prod_serv/products/oc/en/control_solution/ppc_markviedcs_cs.h



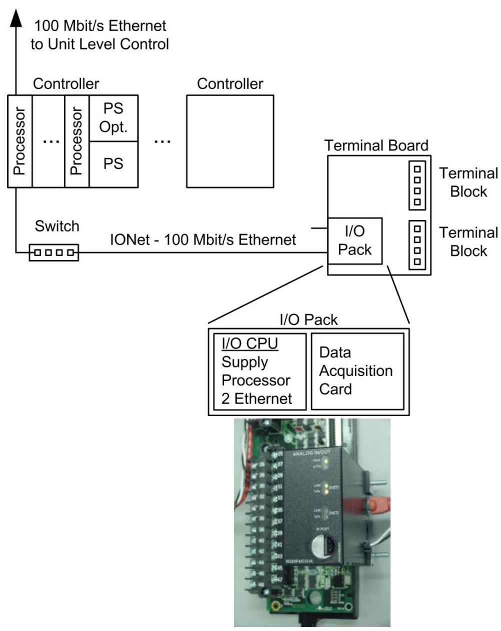
GE Prior Architecture- Centralized



Issues:

1. Signal conditioning problems
2. Inflexible, hard to expand
3. Backplane bandwidth limitations
4. BUT! Customers were familiar with the architecture

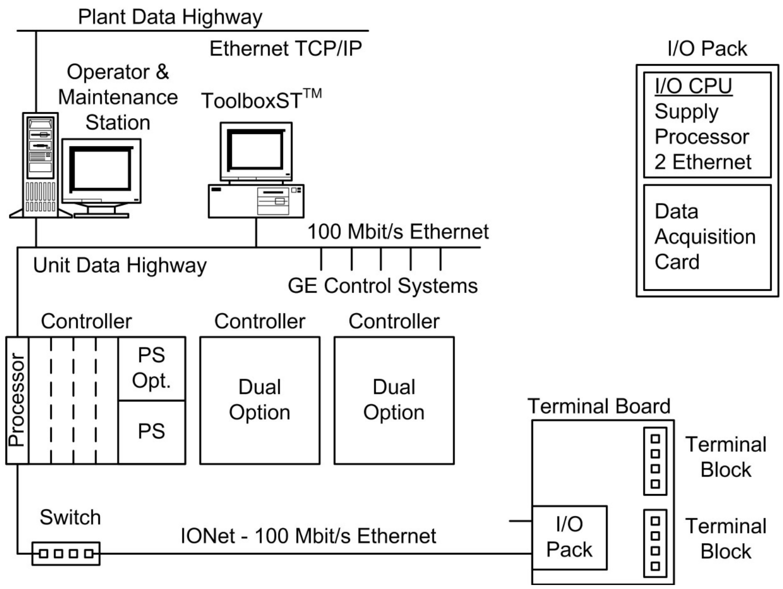
GE New Architecture- Distributed



Issues:

1. SOLVED-Signal conditioning problems
2. SOLVED-Inflexible, hard to expand
3. SOLVED-Backplane bandwidth limitations
4. BUT! Customers were **unfamiliar** with the architecture

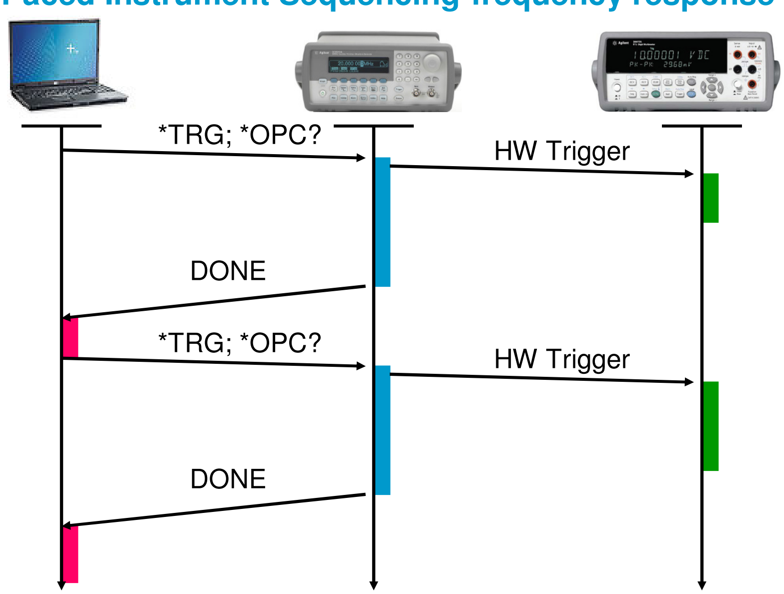
GE New Overall Architecture- Distributed



EECS-149

Slide 15 April 29, 2009

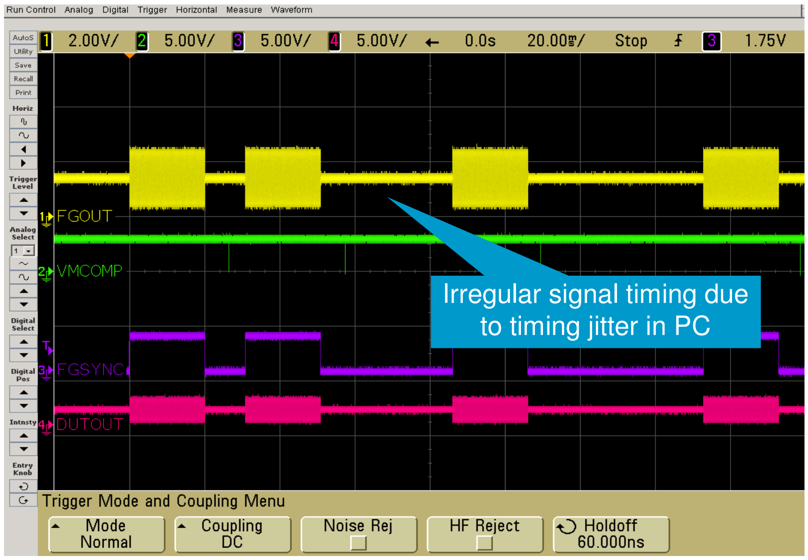
PC Paced Instrument Sequencing-frequency response



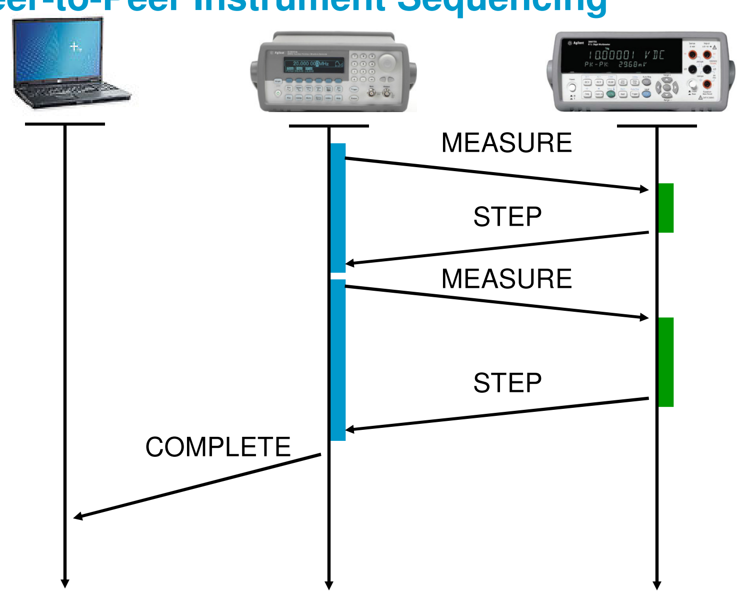
EECS-149

Slide 16 April 29, 2009

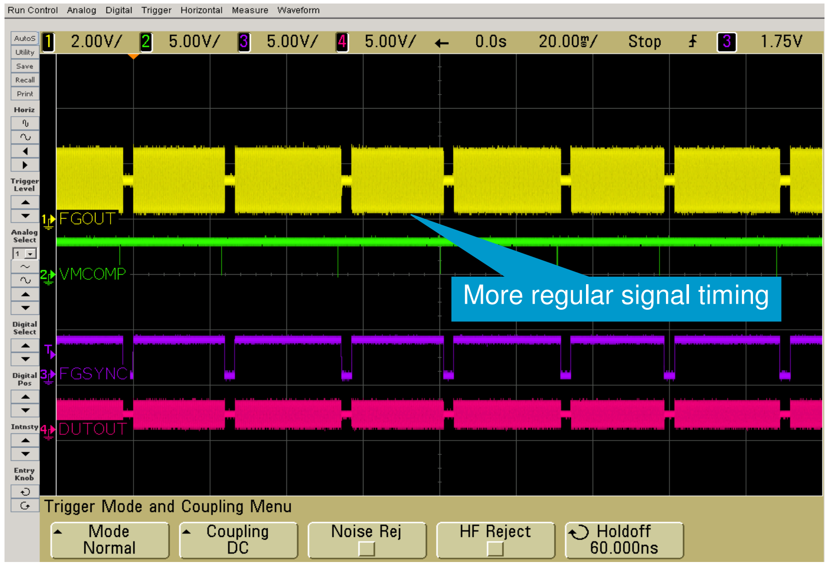
Instrument Sequencing by PC (Baseline)



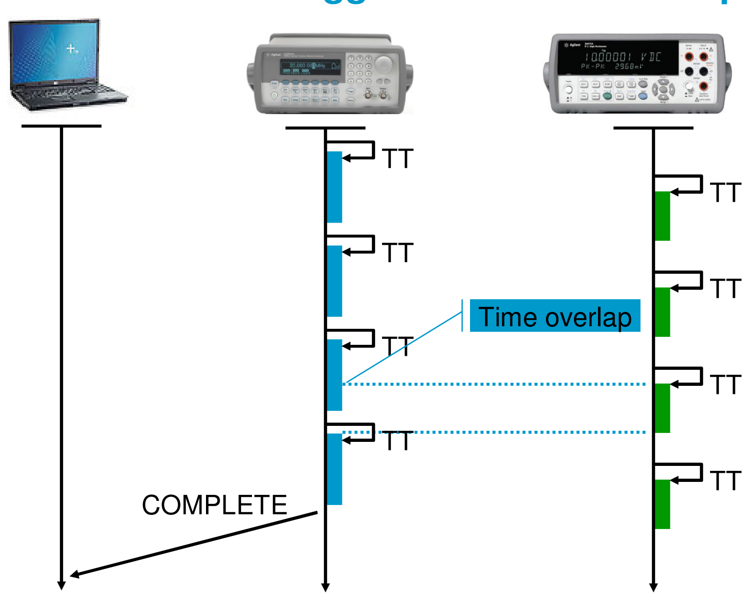
Peer-to-Peer Instrument Sequencing



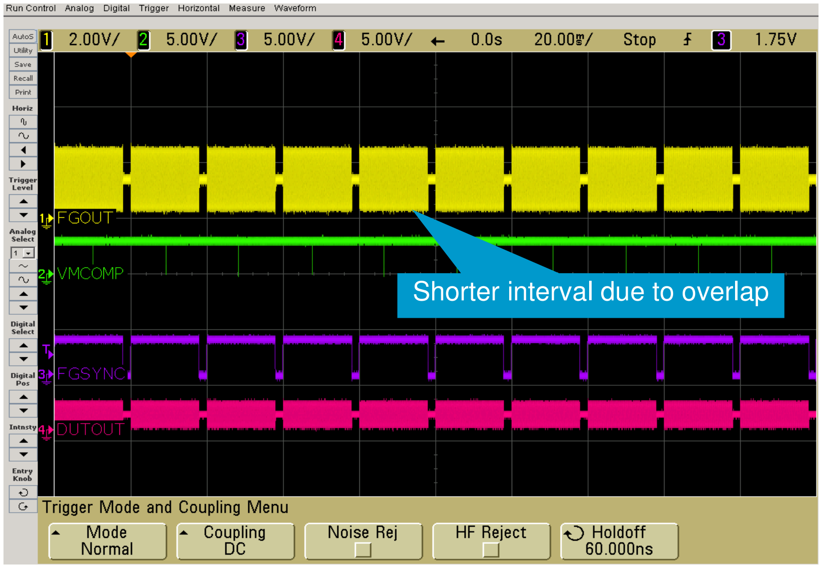
Instrument Sequencing by P2P Messages



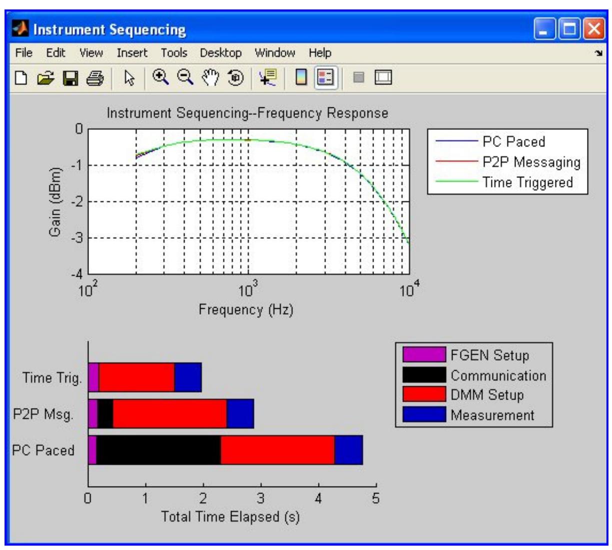
LXI Class B: Time-Triggered Instrument Sequencing



Instrument Sequencing by Time-Triggers



Sequencing to measure frequency response



How does IEEE 1588 Work?

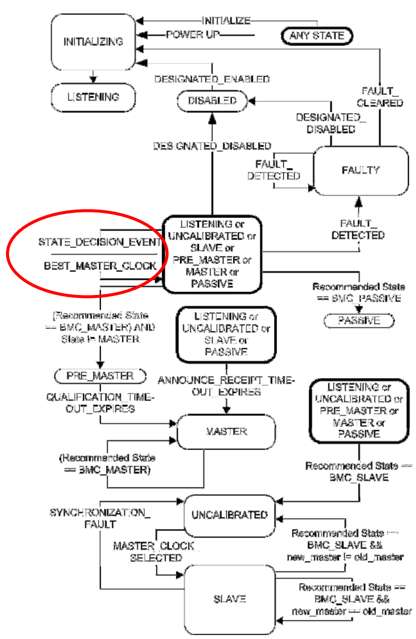
The IEEE 1588 protocol is:

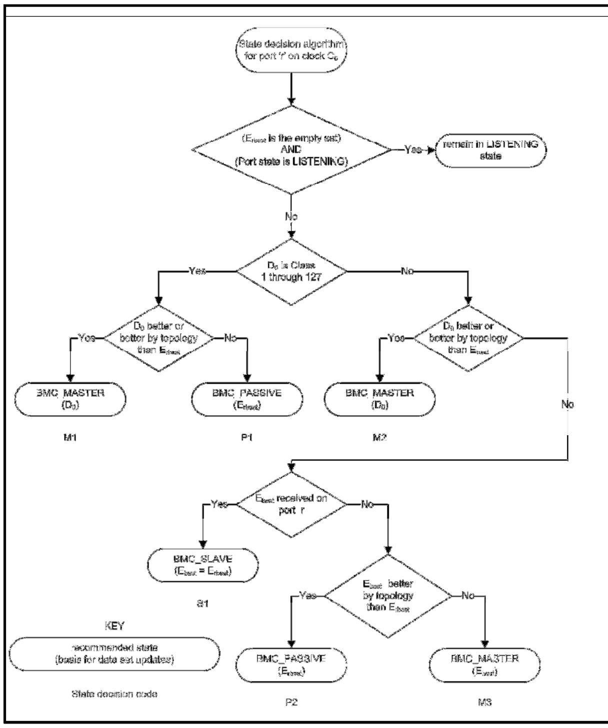
1. Self- assembling
2. Completely distributed
3. Based on the exchange of well defined network messages.

There are two phases of the protocol:

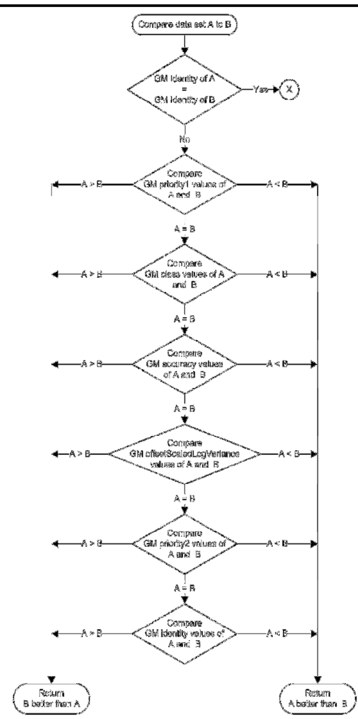
1. Initialization (or reconfiguration): Create a master-slave hierarchy with the ‘best’ or a ‘designated’ clock- the grandmaster- at the root of the tree.
2. Each slave then repeatedly synchronizes to its master.

Initialization or reconfiguration of the master-slave hierarchy.



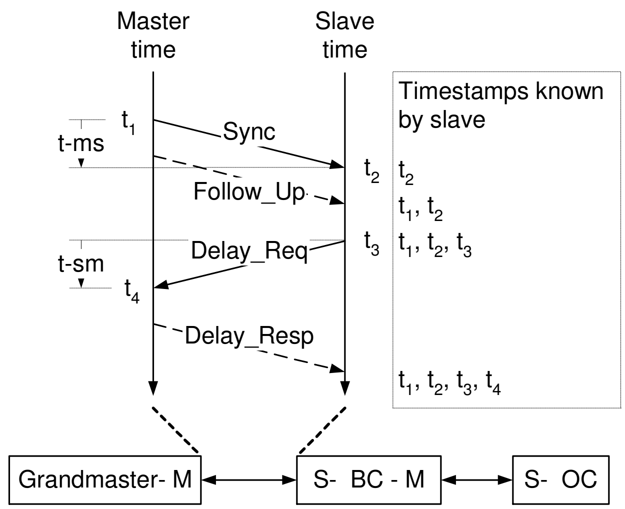


Initialization or reconfiguration of the master-slave hierarchy.



Initialization or reconfiguration of the master-slave hierarchy (2)

Synchronization Basics – Delay Request-Response Mechanism



Synchronization Basics – Delay Request-Response Mechanism - 2

Under the assumption that the link is symmetric

Offset = (Slave time) – (Master time) = $[(t_2 - t_1) - (t_4 - t_3)]/2$ = [(t-ms) – (t-sm)]/2

(propagation time) = $[(t_2 - t_1) + (t_4 - t_3)]/2$ = [(t-ms) + (t-sm)]/2

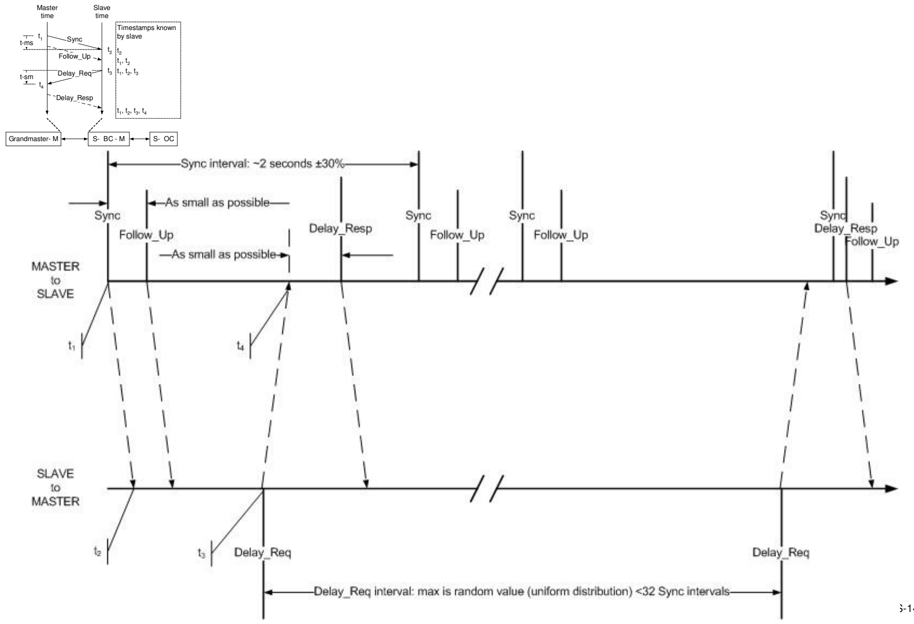
Can rewrite the offset as

Offset = $t_2 - t_1$ – (propagation time) = (t-ms) – (propagation time)

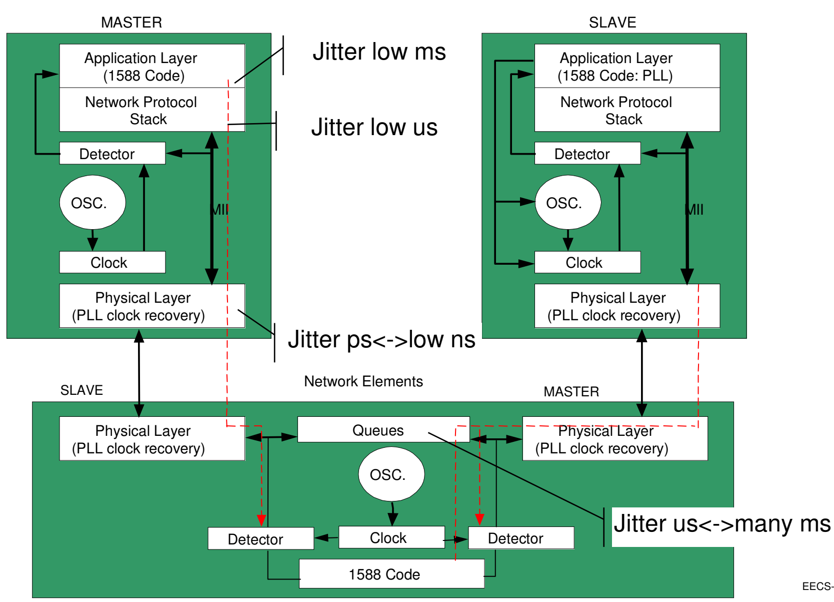
If the link is not symmetric

- The propagation time computed as above is the mean of the master-to-slave and slave-to- master propagation times
- The offset is in error by the difference between the actual master-to-slave and mean propagation times

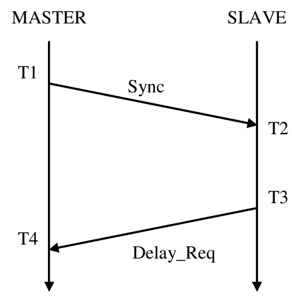
Critical implementation details- message view

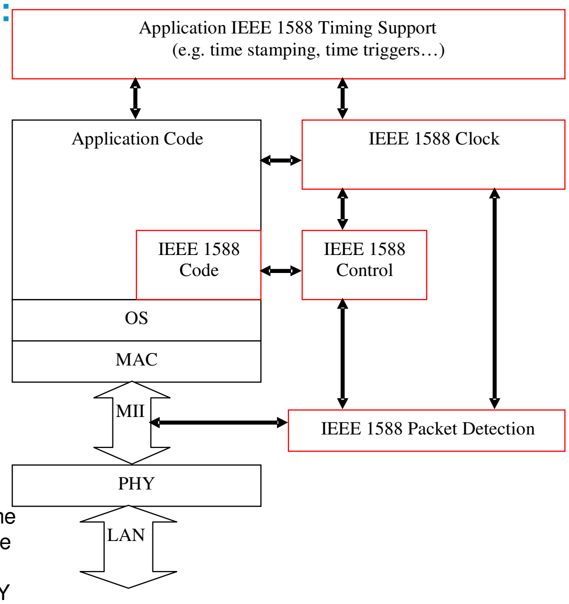


Critical implementation details- network view



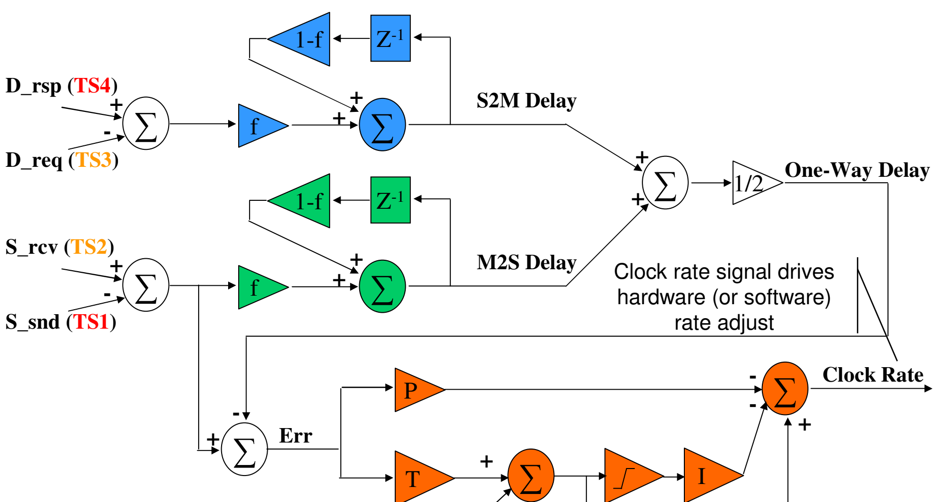
Critical node details:





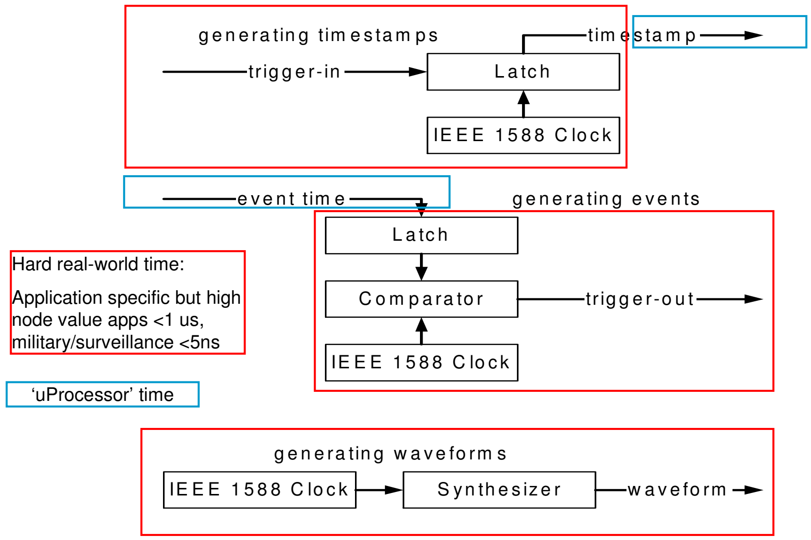
There are PRET design issues! The specifics differ depending on where the 1588 components are located, e.g. at task, ISR, MII, or in the PHY or some combination thereof!

Clock Rate Servo (Software portion)



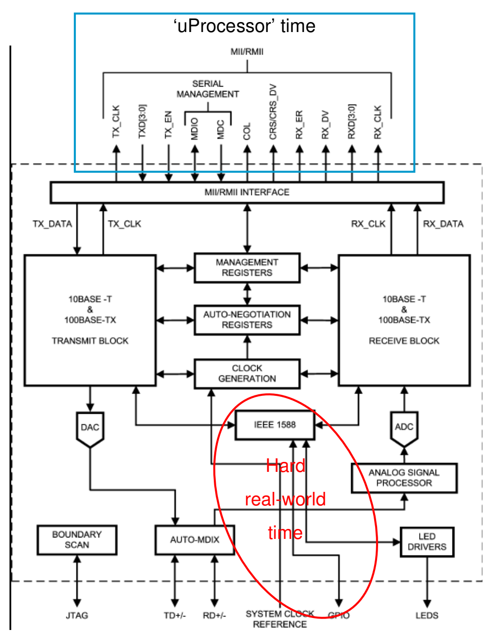
This is a closed loop control system so loop time does matter- hence a PRET design issue!

Coupling IEEE 1588 to your application: Critical issues



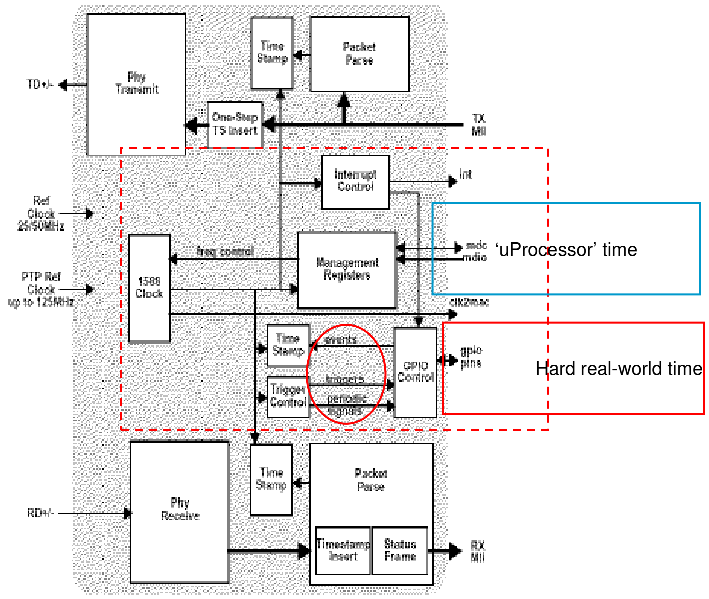
National Semiconductor DP83640 PHYTER

(from DP83640 datasheet)



National Semiconductor DP83640 PHYTER

Simple, Accurate Time Synchronization in an Ethernet Physical Layer Device, David Rosselot, ISPCS 2007



How well can you synchronize?

From: "DP83640 Synchronous Ethernet Mode: Achieving Sub-nanosecond Accuracy in PTP Applications, National Semiconductor Application Note 1730, David Miller, September 2007

SyncE Enabled	Measured Quantity	Mean	Standard Deviation	Peak-to-peak
No	10 MHz clock output	-2.148 ns	5.237 ns	48.3 ns
Yes	10 MHz clock output	319 ps	80.6 ps	900 ps
Yes	1 pulse per second output	1.005 ns	2.8 ps	2.02 ns

Websites

General IEEE 1588 site: contains product pointers, conference records, general guidance, standards related

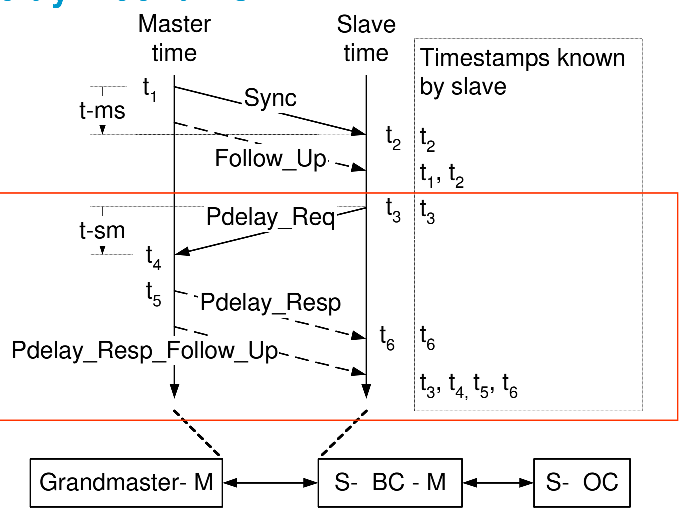
http://ieee1588.nist.gov/

ISPCS (International IEEE Symposium on Precision Clock Synchronization) site: Conference on IEEE 1588 and related subjects

http://www.ispcs.org/

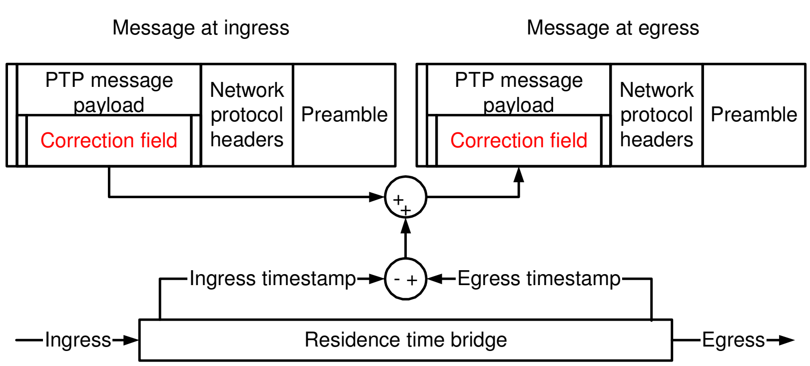
BACKUP SLIDES

Synchronization Basics – Peer Delay Mechanism



End-to-End Transparent Clocks

The residence time is accumulated in a field of the Sync (one-step clock) or Follow_Up (two-step clock) messages



Products (partial listing)

Infrastructure:

- Boundary and transparent clocks (IEEE 1588 bridges): Hirschmann, Westermo, Cisco, others
- GPS master clocks: Symmetricom, Meinberg, Westermo,…

Silicon:

- Microprocessors with embedded 1588: Intel, Hyperstone, Freescale, AMCC,…
- PHY/MAC level: National Semiconductor, others in proto or 1st silicon (some also implement synchronous Ethernet)

Protocol & misc:

- 1588 stacks, IP blocks, consulting: IXXAT, U. Zurich, MoreThanIP, others
- Wireshark

Audio/video systems applications

Consumer electronics: IEEE 802.1as

http://www.ieee802.org/1/pages/802.1as.html

The "AVB" effort should be carefully investigated by both PTIDES and PRET.