FORMLESS: Scalable Utilization of Embedded Manycores in Streaming Applications

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**Throughput Estimation:**
Theorem: Assuming large inter-processor buffers, for any task assignment of dataflow graph G to P processors, there exists an ordering of tasks on processors such that every precedence constraint is met (possibility by overlapping iterations), and the steady state execution period (inverse of throughput) of the application is \( EP = \max\{\text{workload}(p)\} \).

**Task Assignment**
- Objective: minimize execution period EP
- Constraint: each processor should have at most 4 connections from and 4 connections to other processors
- Implementation: METIS graph partitioning software
- Post partitioning adjustment to meet the above constraint

**Local Scheduling**
- Overlap execution of different iterations of the application tasks
- Must respect the dependencies
- Increases throughput
- Increases memory requirement for inter-task buffers

**Baseline Software Synthesis**

**Design Space Exploration**

**FORMLESS Application**

**Instatiated Task Graph**

**Task Assignment**

**Task Profiling**

**SEAM Simulator**

**FPGA Prototyped Platform**
- Altera DE4 FPGA board
- 16 NiosII cores
- Instruction cache: 6KB
- Data cache: 32KB
- FIFO depth: 1024

Advanced Encryption Standard (AES)

Low Density Parity Check (LDPC)

Matrix Multiply