Timing Analysis of Embedded Software for Families of Microarchitectures

Jan Reineke, UC Berkeley

Edward A. Lee, UC Berkeley

Representing Distributed Sense and Control Systems (DSCS) theme of MuSyC

Clark Kerr Campus, UC Berkeley

November 17, 2011

With thanks to:
Hiren Patel
Alberto Sangiovanni-Vincentelli

This work has received funding from NSF #0720882 and MURI #FA9550-06-0312.
The Challenge: Microarchitecture Selection

// Perform the convolution.
for (int i=0; i<10; i++) {
  x[i] = a[i]*b[j-i];
  // Notify listeners.
  notify(x[i]);
}

Select a microarchitecture that
a) satisfies all timing requirements, and
b) minimizes cost/size/energy.

Choices:
- Processor frequency
- Sizes and latencies of local memories
- …

Family of Microarchitectures
= Platform

Timing Requirements
Timing Analysis Today

- Timing Requirements
- Software Binary
- Timing Model
- Micro-architecture
What does the execution time of a program depend on?

**Input-dependent control flow**

**Microarchitectural State**

- Complex CPU
- L1 Cache
- L2 Cache
- Main Memory

Pipeline, Memory Hierarchy, Interconnect
Example of Influence of Microarchitectural State

x = a + b;
LOAD r2, _a
LOAD r1, _b
ADD r3, r2, r1

Motorola PowerPC 755

Execution Time (Clock Cycles)

Best Case  Worst Case

Courtesy of Reinhard Wilhelm.
Reineke et al., Berkeley 5
1. For every microarchitecture ➔ a different timing model
   time-consuming, costly, error-prone, and still often inaccurate
2. Space of microarchitectures and their configurations is huge
How it will be done tomorrow: Start out with the Timing Model

Reverse process:
1. Design platform timing model for precise and efficient timing analysis.
2. Develop family of microarchitectures conforming to this model.

But one platform timing model will not fit all realizations of the platform!
Support Wide Range of Realizations: Parameterize the Timing Model

1. Parameterize the model to enable wide range of realizations.
2. Parametric timing analysis: symbolic computation of *all microarchitectures* that satisfy the timing requirements.
Example of Parameters and Analysis Results: WCET in Terms of Parameters

Assume four parameters:
1. Presence/absence of floating-point unit
2. Size of cache $|\text{cache}|$ in bytes
3. Processor period $p=1/$frequency in nanoseconds
4. Latency of main memory $l$ in nanoseconds

\[
\begin{align*}
\text{WCET} &= 10*p + 3*l \\
\text{WCET} &= 12*p + 3*l \\
\text{WCET} &= 13*p + 5*l \\
\text{WCET} &= 15*p + 5*l
\end{align*}
\]
Example of Analysis Results: Assume Deadline D

This enables us to determine the cheapest/most-energy efficient/… microarchitecture satisfying the constraints!
Related Challenge: Configuration at Runtime

Microarchitecture selected at design time eliminates some of the options, but not necessarily all:

Given a model of the power consumption of the processor, we can derive energy optimal cache and processor configurations in terms of the deadline.

Reineke et al., Berkeley 11
Related Challenge: Configuration at Runtime

Microarchitecture selection is based on worst-case assumptions at design time. At runtime we may have more knowledge:

\[ e = (\text{time}, \text{input}) \]
\[ e' = (\text{time} + \text{ET}(\text{A, input}), \text{input'}, \text{deadline}) \]

Execution time \( \text{ET}(\text{A, input}) \) may be less than worst-case execution time \( \text{WCET}(\text{A}) \).

Deadline may be greater than deadline assumed at design time.

We can exploit this knowledge to reconfigure a microarchitecture at runtime:

- Frequency/voltage scaling
- Distribution of shared resources:
  - Shared cache/scratchpad
  - Functional units
Parameterized Timing Models: Formalization

Execution time of program P under input i

Parameters

Program P
Input i

Worst case over all inputs

\[ ET_{P,i}(\pi_1, \ldots, \pi_n) : \mathbb{R}^n \rightarrow \mathbb{R} \]

\[ WCET_P(\pi_1, \ldots, \pi_n) := \max_{i \in I} ET_{P,i}(\pi_1, \ldots, \pi_n) \]
Necessary and Desirable Properties of Parameterized Timing Models

**Necessary:**
Execution time should be monotone in parameters.

“a higher frequency always yields a shorter execution time”
“a smaller cache always yields a longer execution time”

**Desirable for efficiency:**
Execution time should depend linearly on parameters.

“doubling the processor frequency will decrease execution time by a factor of two”
Parametric Timing Analysis: Black-Box Approach

“Reduce to known problem” and “Generalize from examples”

We know how to select representative parameter valuations.

Exploits properties of parameterized timing models to generalize from samples to parametric formula.
Modern microarchitectures are optimized for average-case performance at the expense of timing predictability and repeatability.

Context: Precision-Timed (PRET) Machines
http://chess.eecs.berkeley.edu/pret/

The goal of the PRET project is to reintroduce timing predictability and repeatability without sacrificing performance.

Instruction Set Architecture:
Precise control over timing through deadline instructions.

Microarchitecture:
The Precision-Timed ARM adheres to a simple timing model without sacrificing performance:
- Thread-interleaved pipeline
- Scratchpad memories in place of caches
- Predictable DRAM controller

Parametric Timing Analysis

Black-box WCET analysis can be realized using GameTime (Sanjit Seshia).
Conclusions and Future Work

- Today, timing models originate from previously developed microarchitectures.

- Tomorrow, timing models will be carefully designed to enable precise and efficient parametric timing analysis, and microarchitectures will follow.

- Ongoing work: Proof-of-concept implementation for a parameterized PRET timing model.